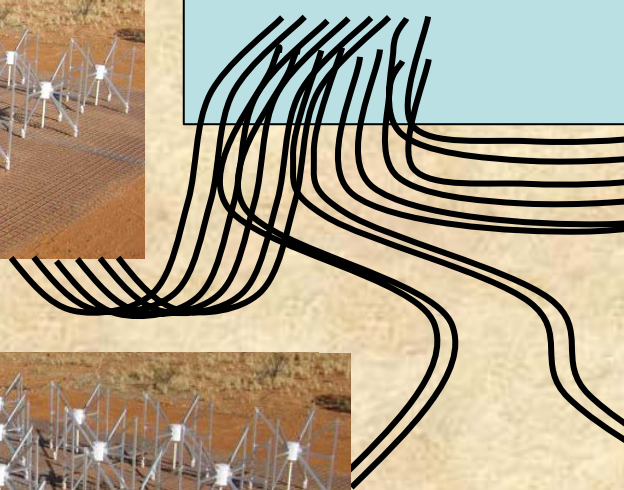
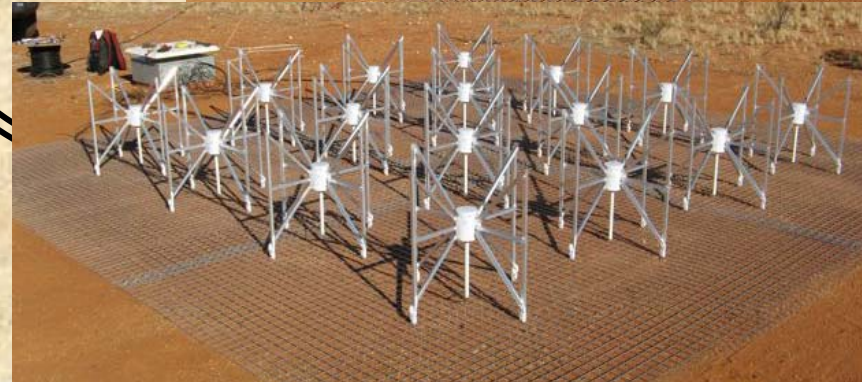
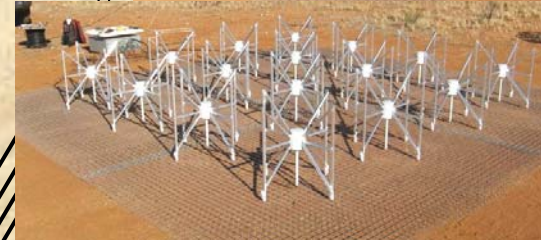
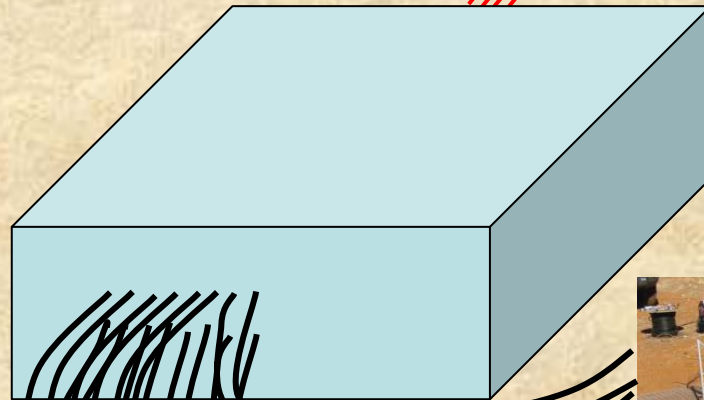
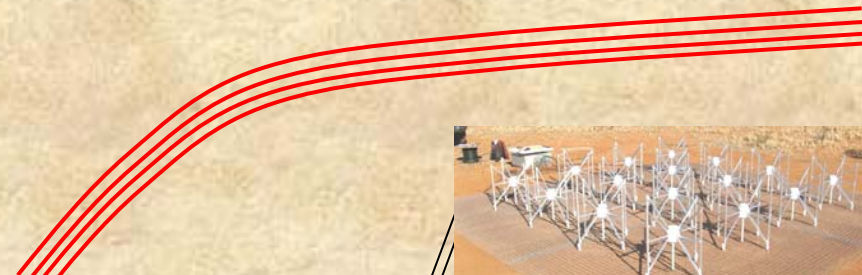
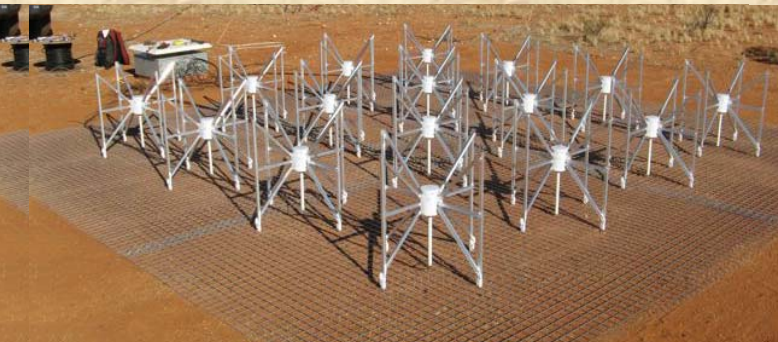


MWA has 64 *Receiver Nodes*

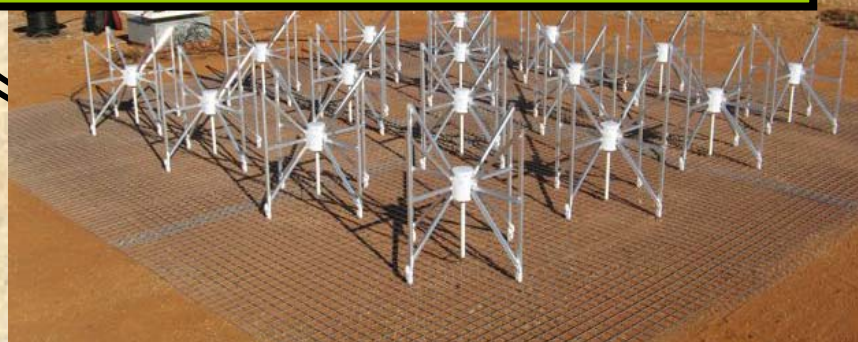
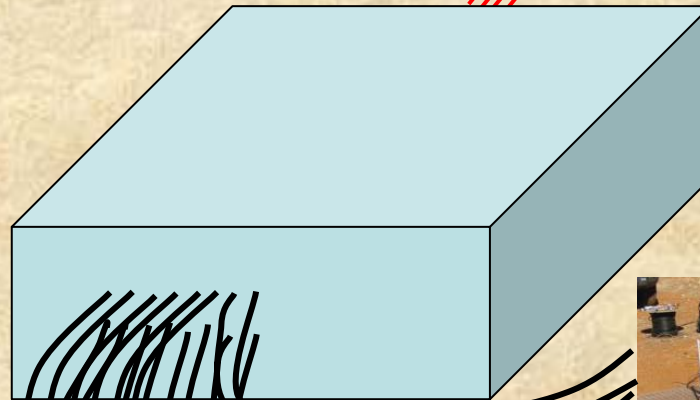
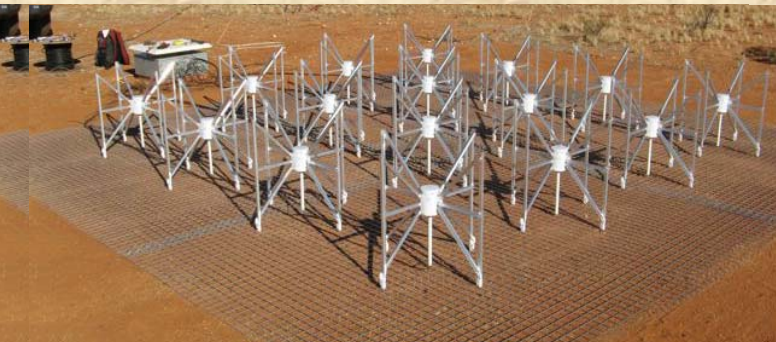


principle *Function* of each node

16 x 32 MHz
digitized output

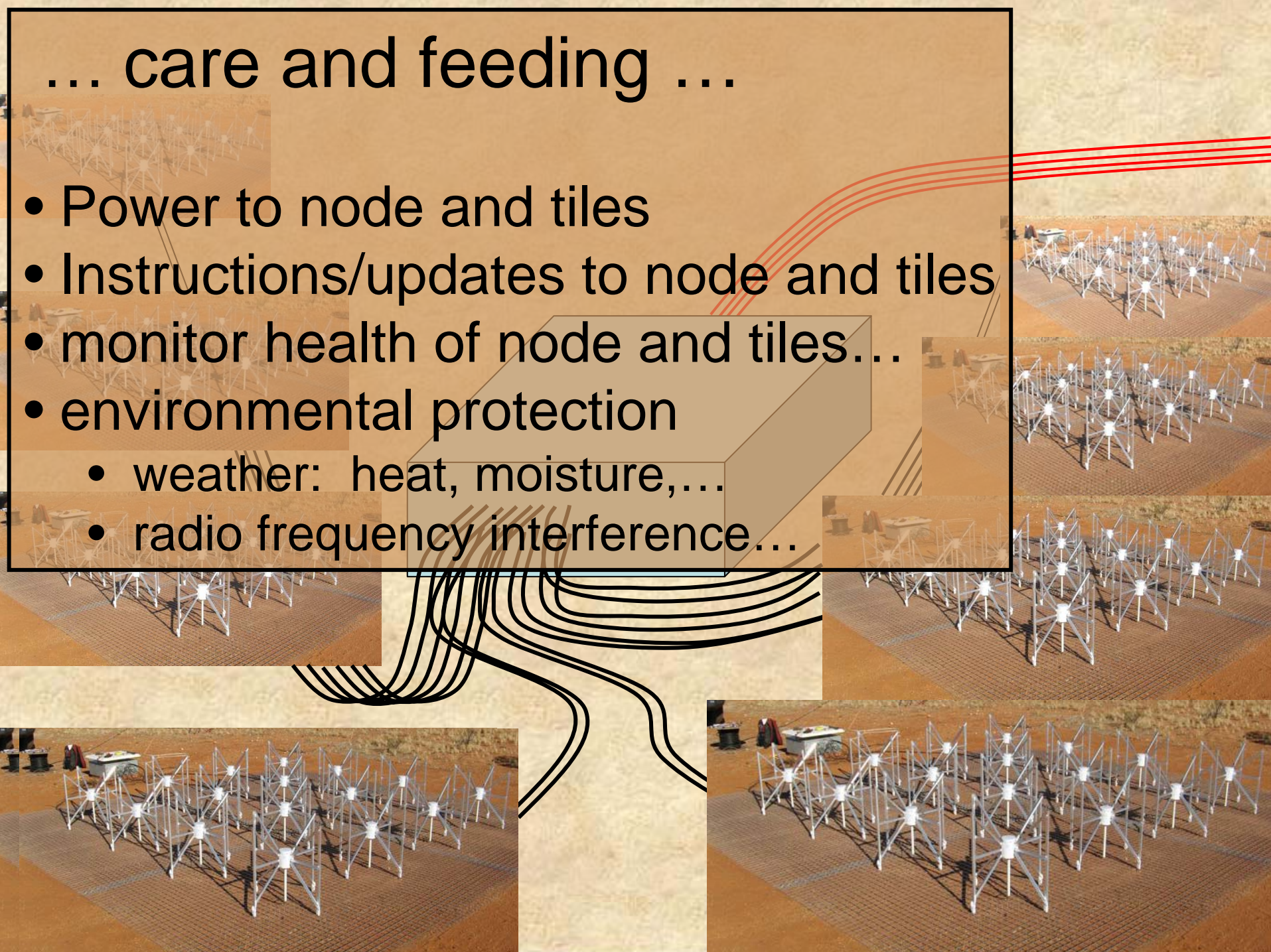
5 Gb/s /Node

16 x 300 MHz RF input



... care and feeding ...

- Power to node and tiles
- Instructions/updates to node and tiles
- monitor health of node and tiles...
- environmental protection
 - weather: heat, moisture,...
 - radio frequency interference...



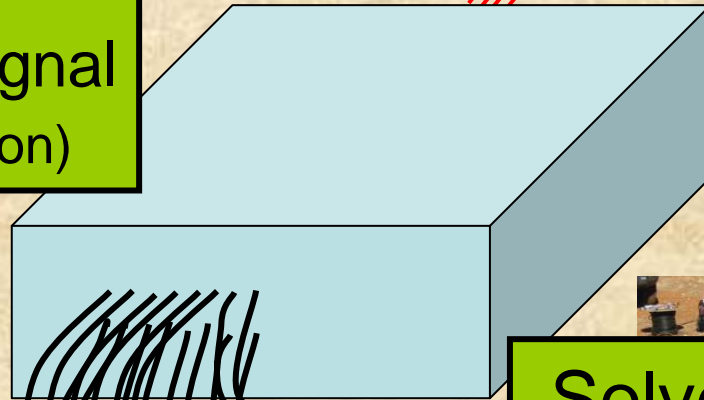
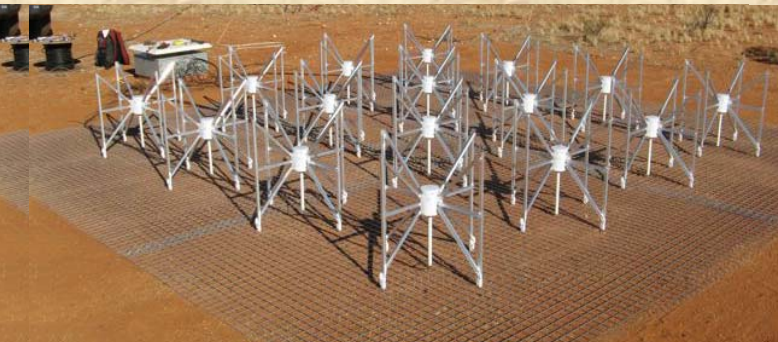
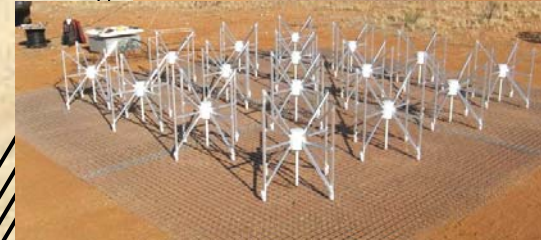
A Significant complexity...

looking to measure “correlation coefficients”

- cross talk
- coupling
- common mode signal
- DC term (ED jargon)

Solved by
Phase-switching

Cycle through 16 orthogonal
Walsh states...



Who ?

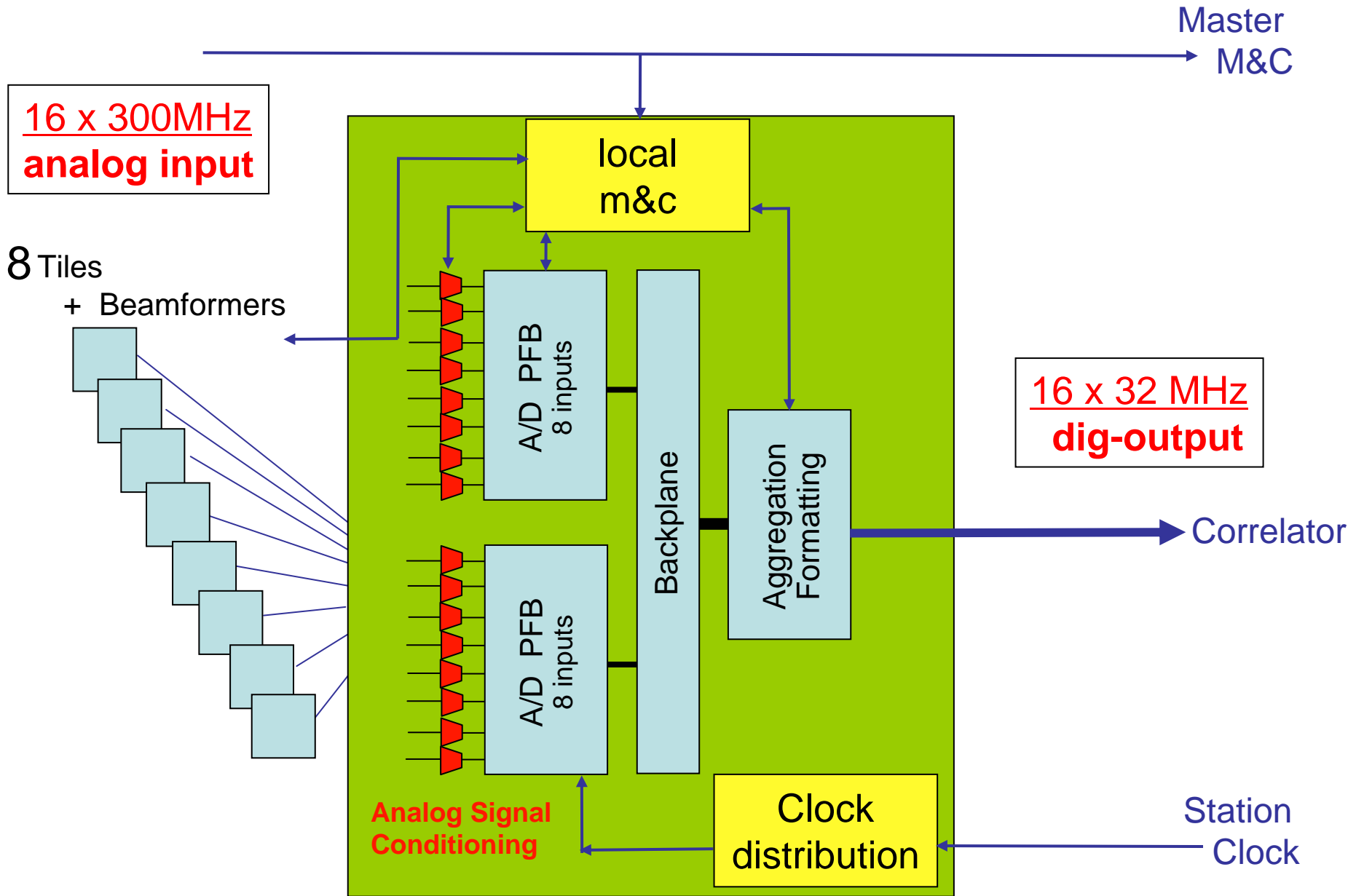
ANU:

- Mark Waterson - WP Manager
- Errol Kowald
- Annino Vaccarella
- (Glen Torr)
- (Jonathon Kocz)
- Frank Briggs

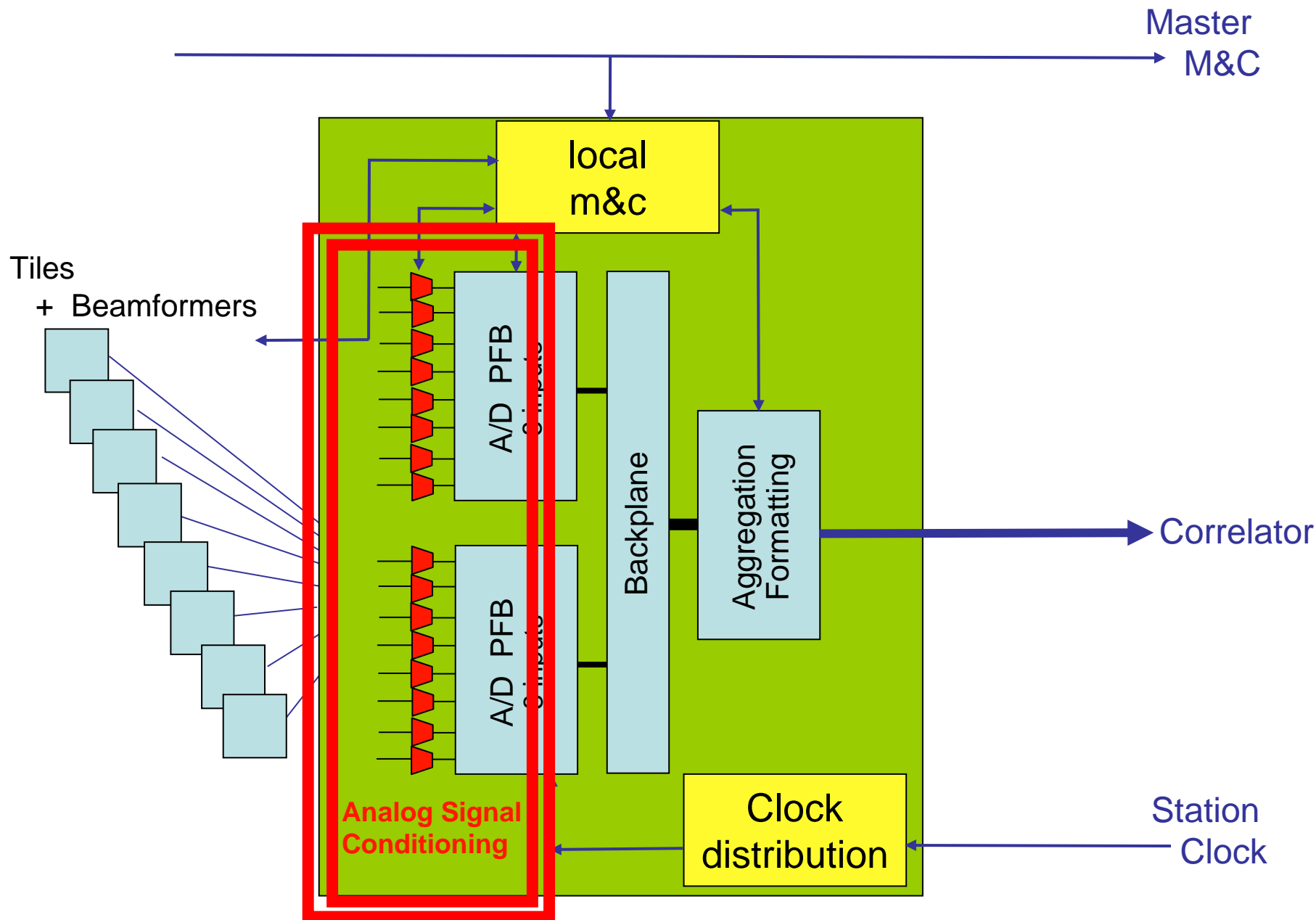
RRI:

- Anish Roshi - RRI coordinator
- Prabu
- Srivani
- Gopal Krishna

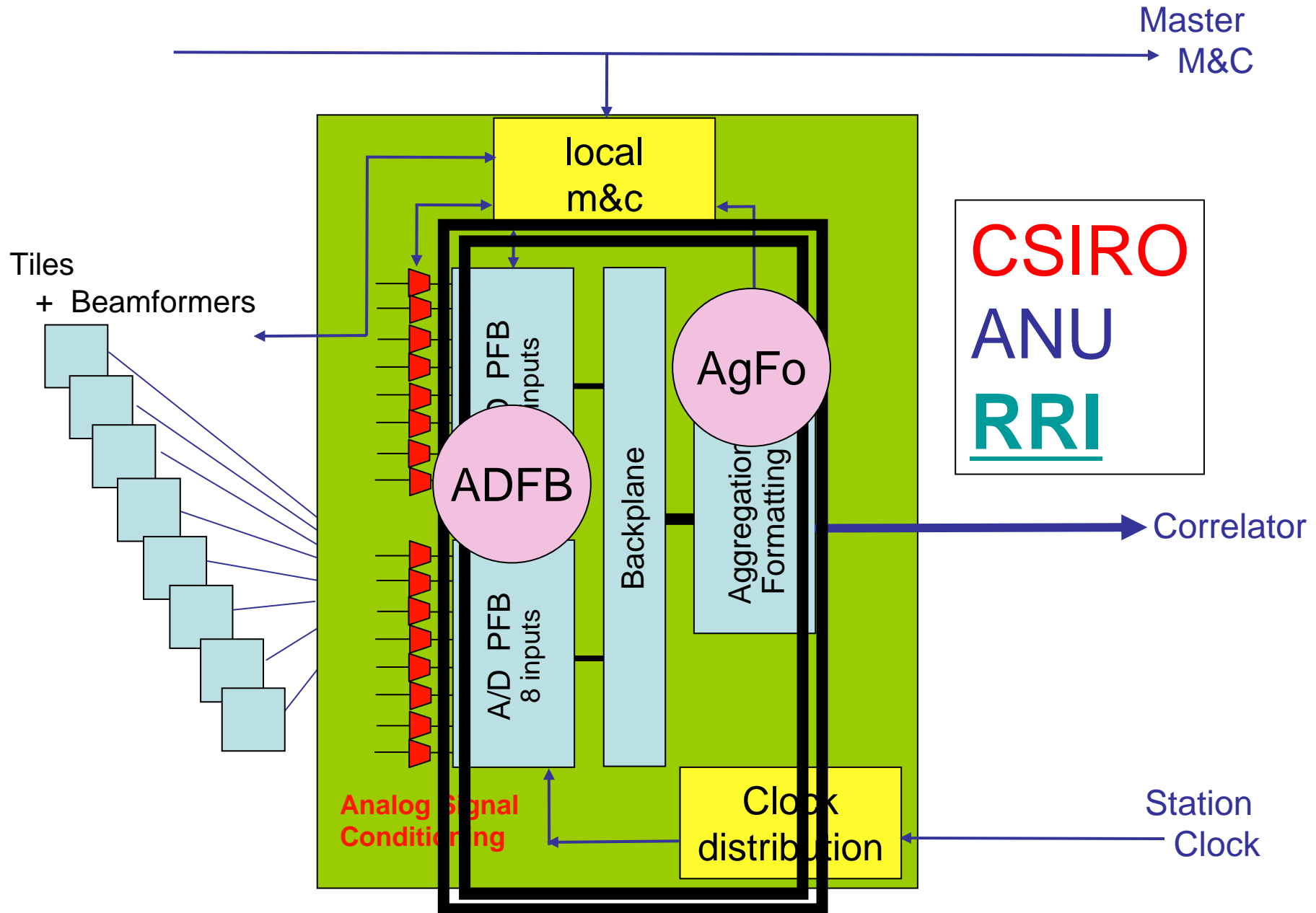
Receiver Node principal components



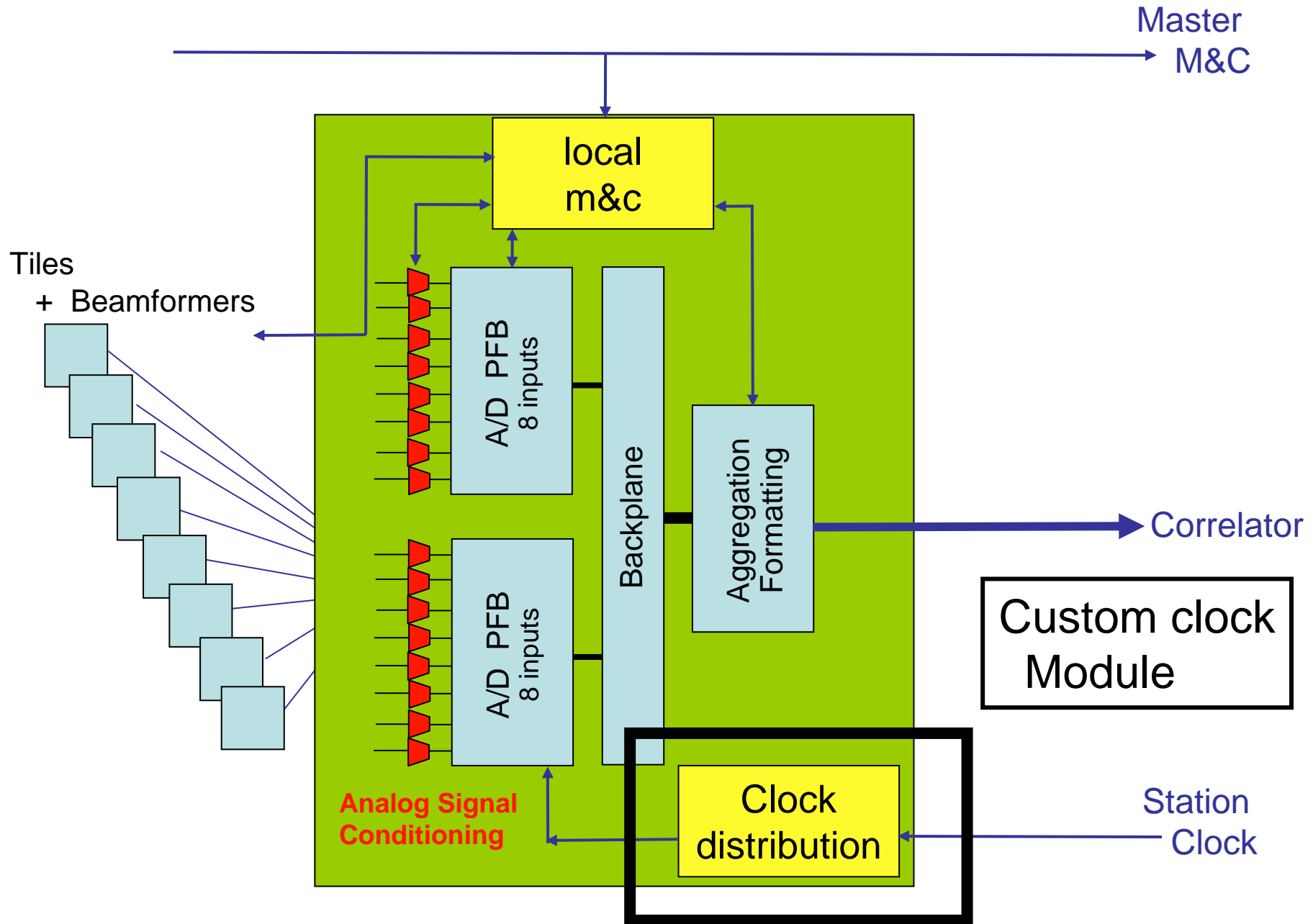
Analog Passband Filters and Amplifiers to adjust Power Levels



High-speed Digital components and synchronization



Sampling clock @660 MHz, plus Synchronization



Projected Schedule for Receiver Development...

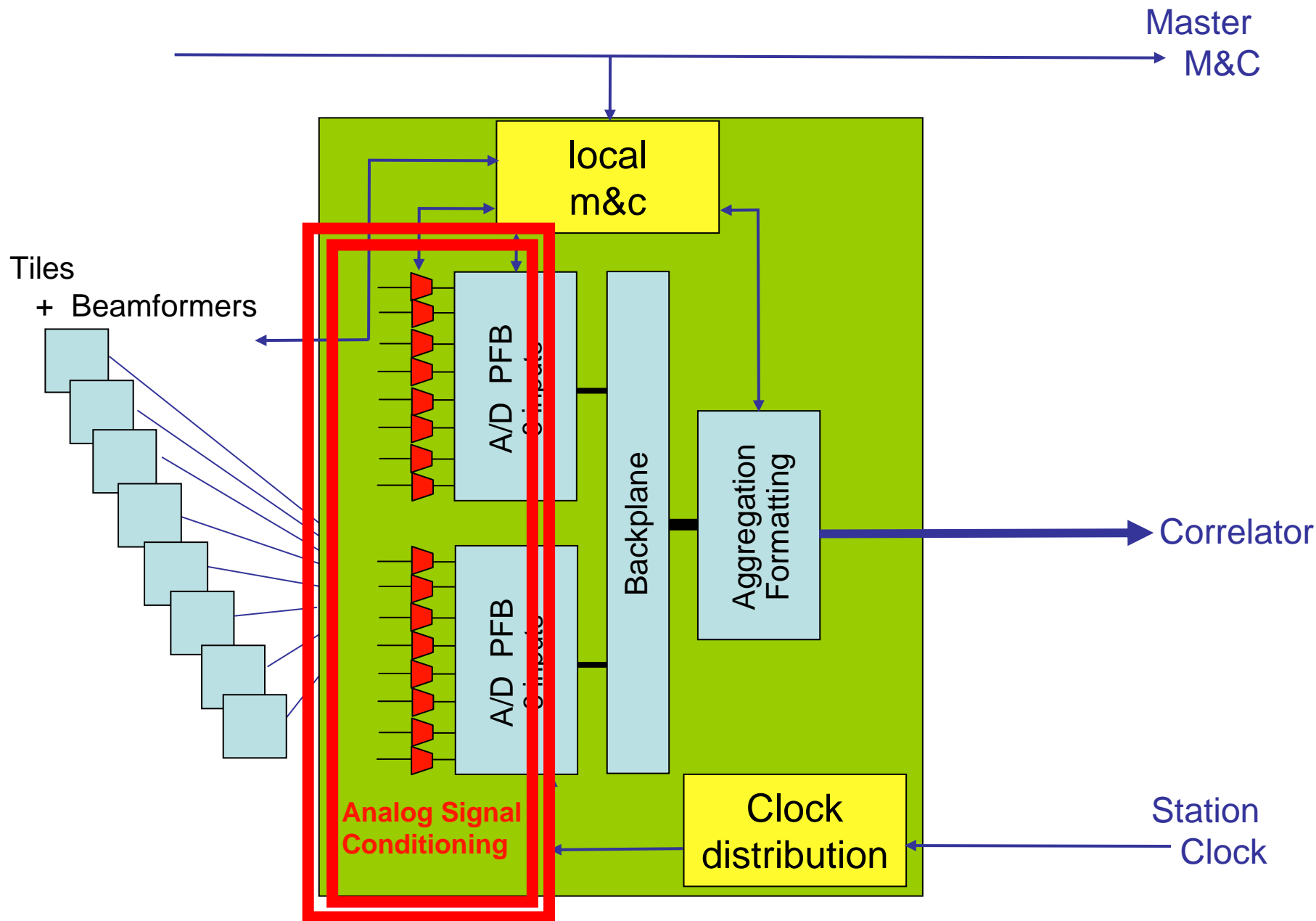
ANU

- core electronics for 1 receiver by 1 September (w/o AgFo)
- 4 receivers in Q4 2007
- packaging by 1 January

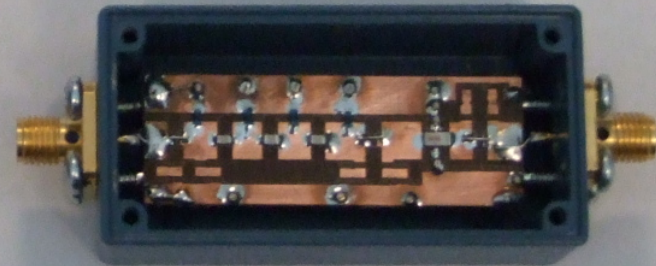
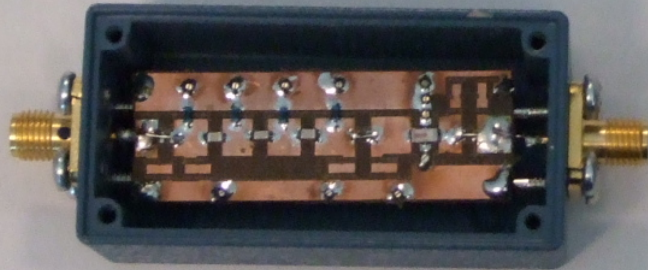
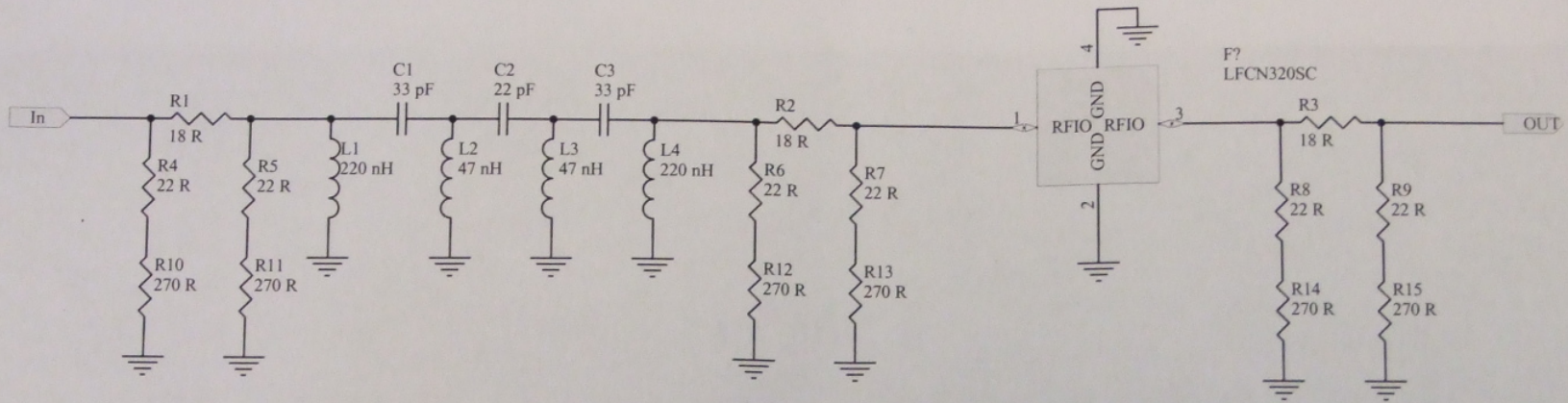
RRI

- simulation of 2xPFB code with ADC interface - end June
- 1 channel ADFB board - early July
- code ready for serial data output - early July
- schematic for AgFo board - end July
- 4 channel ADFB board - early August
- PCB fabrication of AgFo board - end August
- most code ready for node - early September
- 2 fully populated boards - mid September
- testing of AgFo board - mid September
- high-speed digital components ready at RRI - mid October

Analog Passband Filters and Amplifiers to adjust Power Levels



Prototype Passband Filters: shipped 2 to WA for 1T expts (no amplifiers)



Title		
Size	Number	Revision
A		
Date:	23/05/2007	Sheet of
File:	E:\Astro Project II\ASC.SCHDOC	Drawn By:

Ref 0 dBm

Atten 10 dB

500 MHz

Peak
Log
6
dB/

DI
-24.0
dBm

Display Line
-23.98 dBm

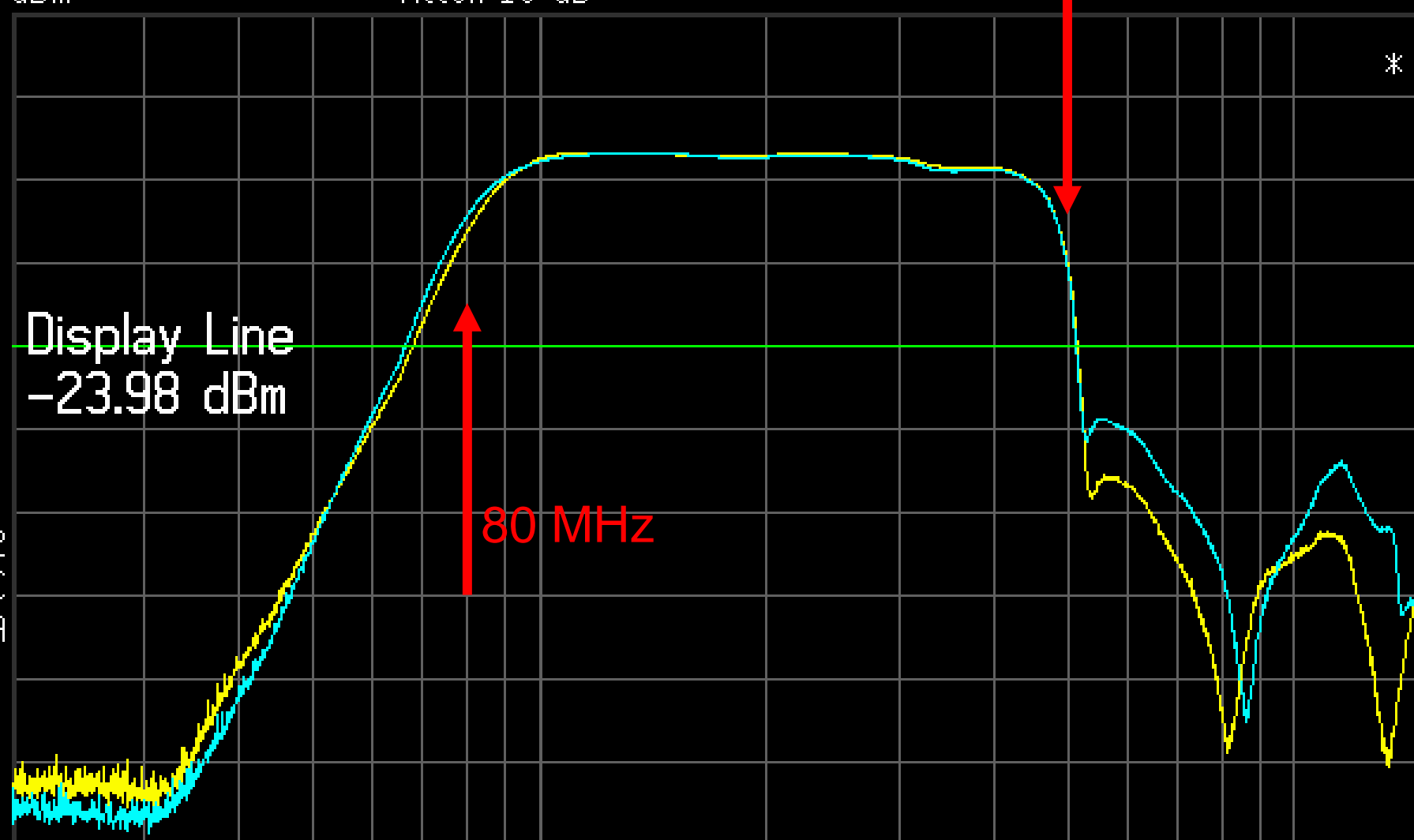
W1 V2
S3 FC
AA

80 MHz

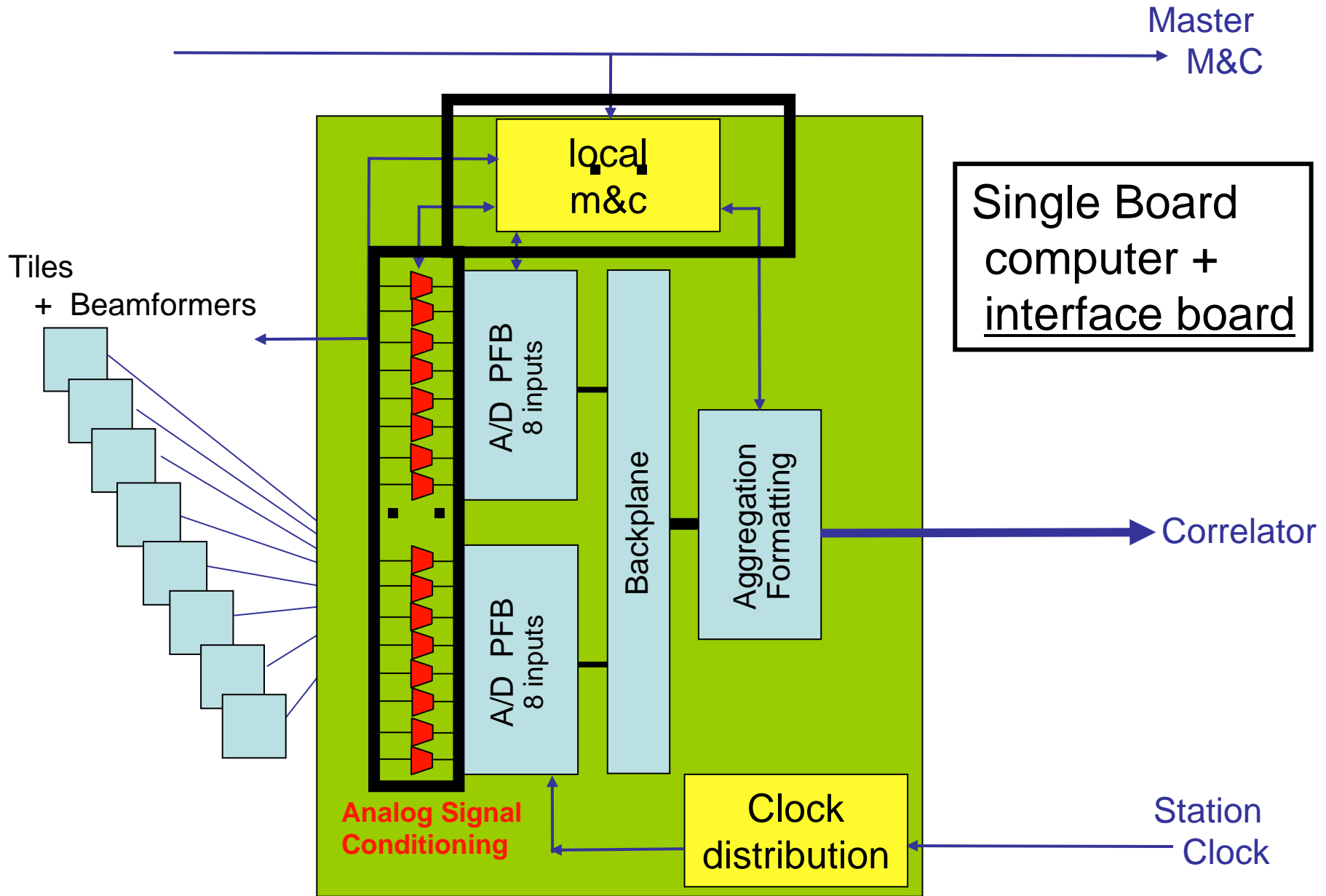
Start 20 MHz
Res BW 3 MHz

VBW 3 MHz

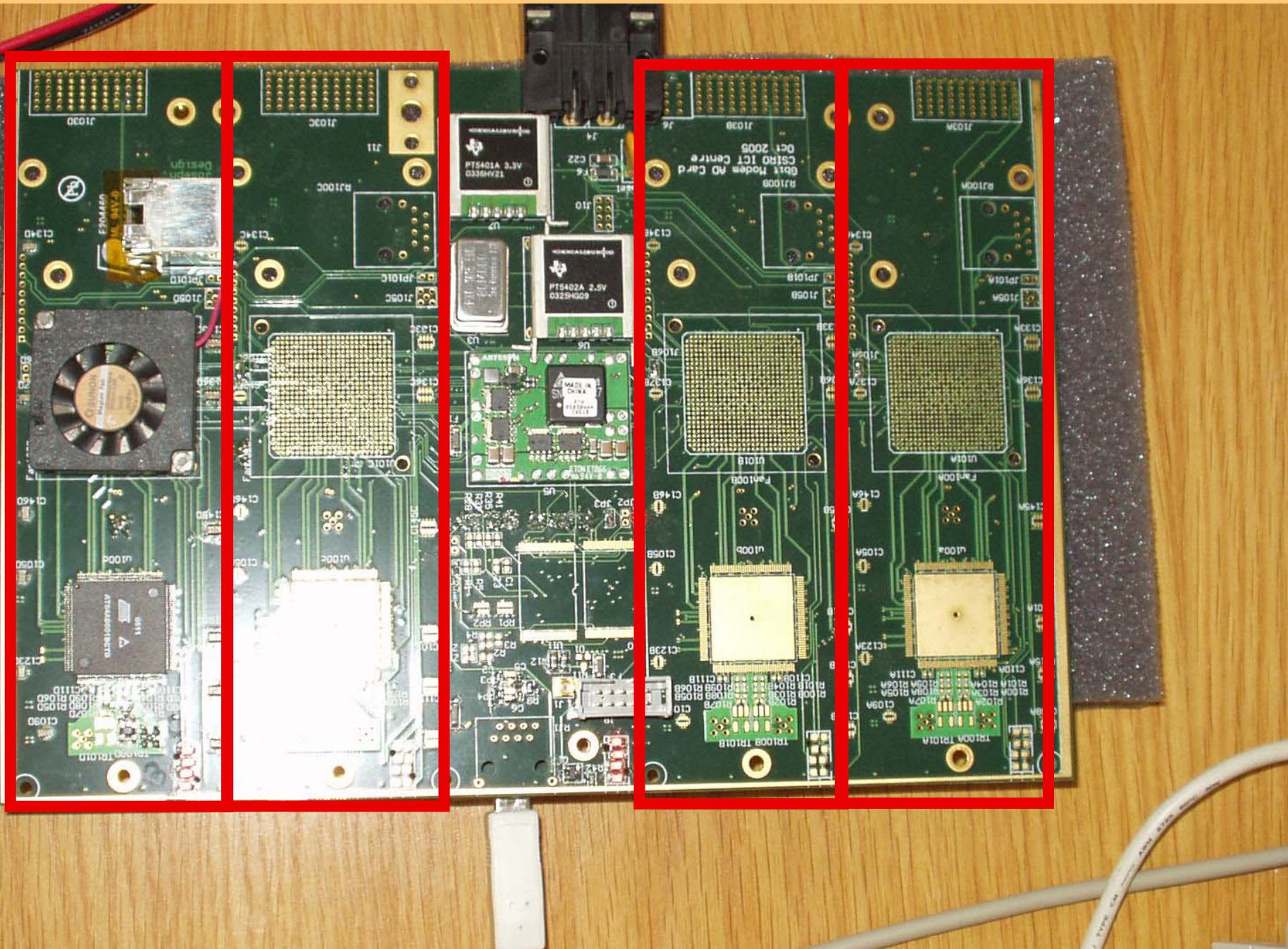
Stop 1.5 GHz
Sweep 550 ms (2497 pts)



M&C ... \Leftrightarrow ... ASC units



CSIRO Gbit Wireless Board: (4 chan of 1 GHz bandwidth)



CSIRO Board: (Reconfigured to 8 input channels of 500 MHz)

← Connection To back plane

↑ 2 X 32 Msamp/s X (2x4 bit cmplx)

← FPGA

↑ 2 X 660 Msamp/s X 8 bit

← A/D

↑ 2 X (0 - 330 MHz analog)



CSIRO Board: (Reconfigurable to 8 input channels of 500 MHz)

PFB Codes ...running in development board

- modified Berkeley PFB from Ludi
- ATNF PFB from Grant

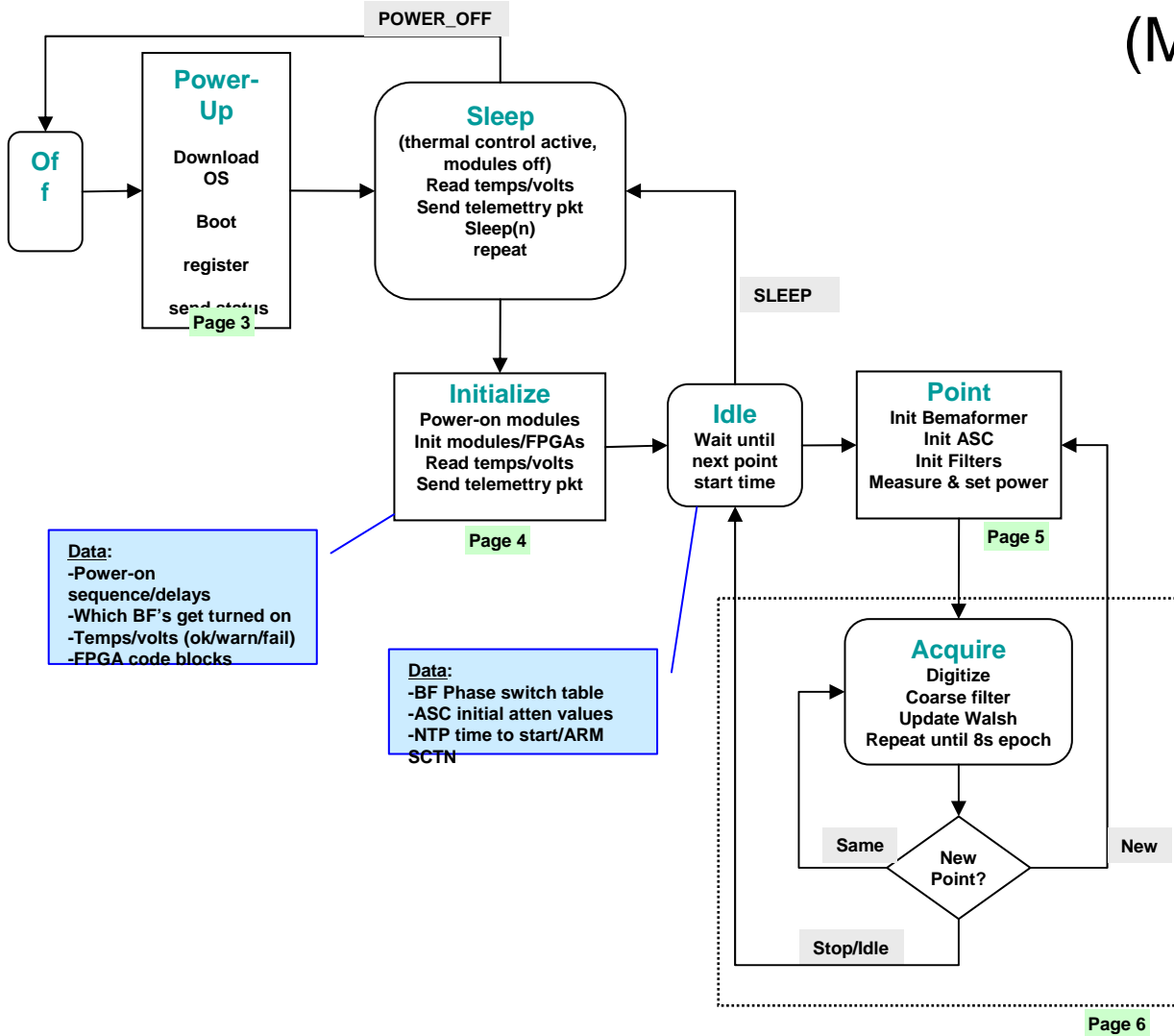
Prototype board...

- partially populated with ADC and FPGA in 1 channel
- shipped to RRI



Overall Receiver Mode/State Transitions

(Mark Waterson)



State Diagram (Anish)

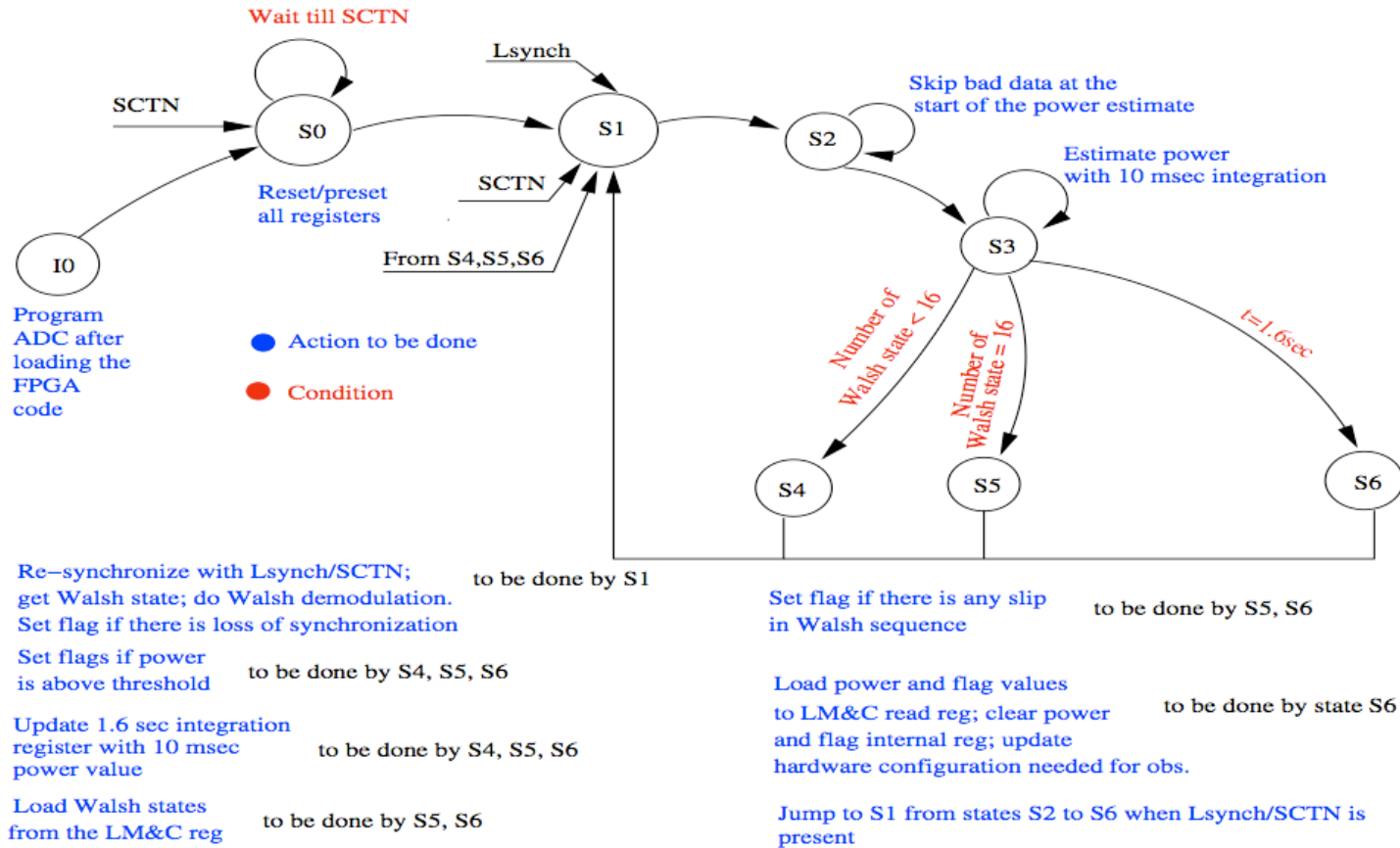


Figure 3: State machine in the ADFB board FPGAs

RRI milestones achieved - from Anish (22 June)

3. Mile Stones Crossed

- Block diagram level design of AgFo ready for discussion
- Block diagram of clock and synchronization requirements for Receiver Node ready for discussion
- Block diagram level design of ADFB firmware ready for discussion
- Simulation of two (Grant's) PFBs + ADC interface is being done; preliminary results on the resource utilization and clock speed are available
- Requirements of the Analog system in the Receiver Node has been worked out and ready for discussion

Projected Schedule for Receiver Development...

ANU

- core electronics for 1 receiver by 1 September (w/o AgFo)
- 4 receivers in Q4 2007
- packaging by 1 January

RRI

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