

Correlation Firmware Status

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PFB Overview

- Ludi deSouza has created a suite of tools for handling both the PFB and CB
 - allows convenient script-driven download of code to all FPGA's
 - provides simple pathway for chip to host PC communications
- Principal building blocks of SKAMP/MWA designs complete and tested
 - PFB
 - Cube rotation (data stream permuter/buffer)
- Potential performance bottleneck could be easily sidestepped by going to 2 PFB boards

PFB Filter

- Ludi has a parameterized model in MATLAB and Perl, that allows one to generate PFB's with specified # taps and filter shape
- Output of model is VHDL code to implement the filter module

Cube Rotator

- permutes order of data, over large time scales (50 - 500 ms)
- also performs buffer function and allows overlapping replay in the PFB
- two different rotations
 - reordering and replay into PFB filters
 - reordering of PFB output into correlator input order
- RAM-based in DDR2 memory (introduces complexity)

Remaining Design Elements

- data packet reception and decoding
- data routing
- adopting cube rotations to MWA parameters
- mesh backplane cross-connect (not done in 32T)
- parameterizing the PFB's for the MWA case
- data packet formation and transmission

PFB Work Plan

- Ludi will continue on SKAMP, Russell McWhirter on MWA, with close interaction
- Sequencing of tasks:
 - PFB already done
 - Input packet reception and decoding
 - Output packet formation and transmission
 - Single coarse channel, skipping rotation, to verify signal processing chain
 - First use only FX-60, then route through whole board
 - Add output cube rotation to allow full 1.28 MHz channel
 - Add input rotations to get all 24 coarse channels

CB Overview

- 32T design complete and verified e2e last Spring
- unanticipated board tweaks and shipping comedy of errors delayed board delivery to 23 October, 2007
- testing further delayed by illness
- hired on Russell McWhirter to compensate
- Ludi de Souza visit in December very helpful

CB Firmware Current Status

- Code download path complete & working
- Code integrated with Ludi's "regbus" infrastructure
- Pathway from gigE PHY chip out working
- Problem du jour is getting clock from PHY to rocket i/o's

CB Work Plan

- verify integrity of gigE output path
- verify that captured correlation data (using prg packets) is same as predicted
- loopback tests to establish input path
- further testing to be described in “System Integration” talk

Additional Work for 512T

- **PFB**

- performance increase only if we use 2 boards for 32 T
- mesh cross-connect via rocket i/o
- different output ordering/packetization

- **CB**

- density of correlation cells
- different signal pair routing
- LTA functionality using DDR2
- different dump rate & packetization
- phased beam functionality