System Overview

MWA/LFD Kickoff Meeting

Roger Cappallo

2006.6.5

LFD General Properties

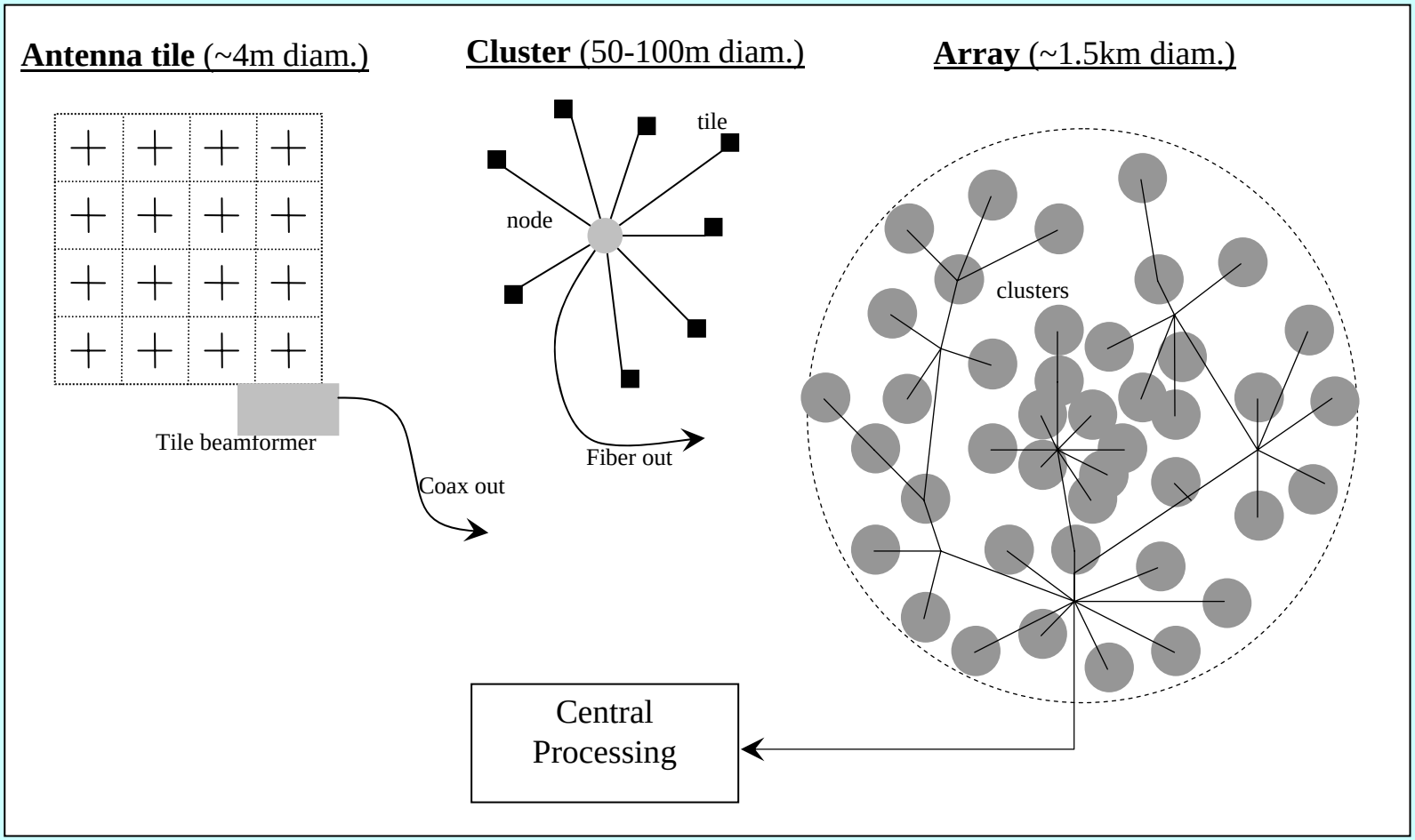
- 500 antenna tiles, 80-300 MHz
  - Each a 4x4 crossed dipole array
  - Electronic analog steering of tile beam
  - Total collecting area ~8000 m^2 at 150 MHz
  - Direct sampling of RF as early as possible
  - 8 bits/sample fine with low RFI environment in Mileura

- Full cross-correlation architecture
  - Simpler, easier, cheaper, *better for wide FOV*
  - Reliance upon DSP advances
  - 32 MHz processed bandwidth
  - Distributed FX architecture, FPGA-based

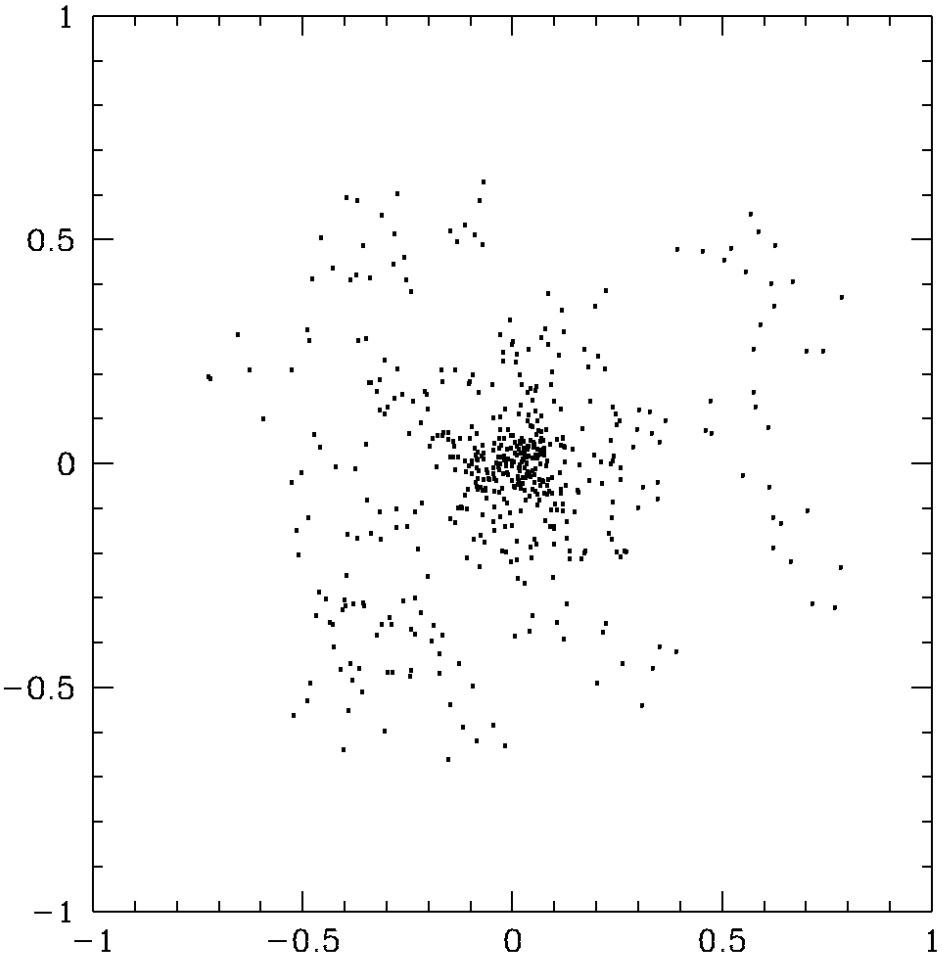
LFD General Properties (cont’d)

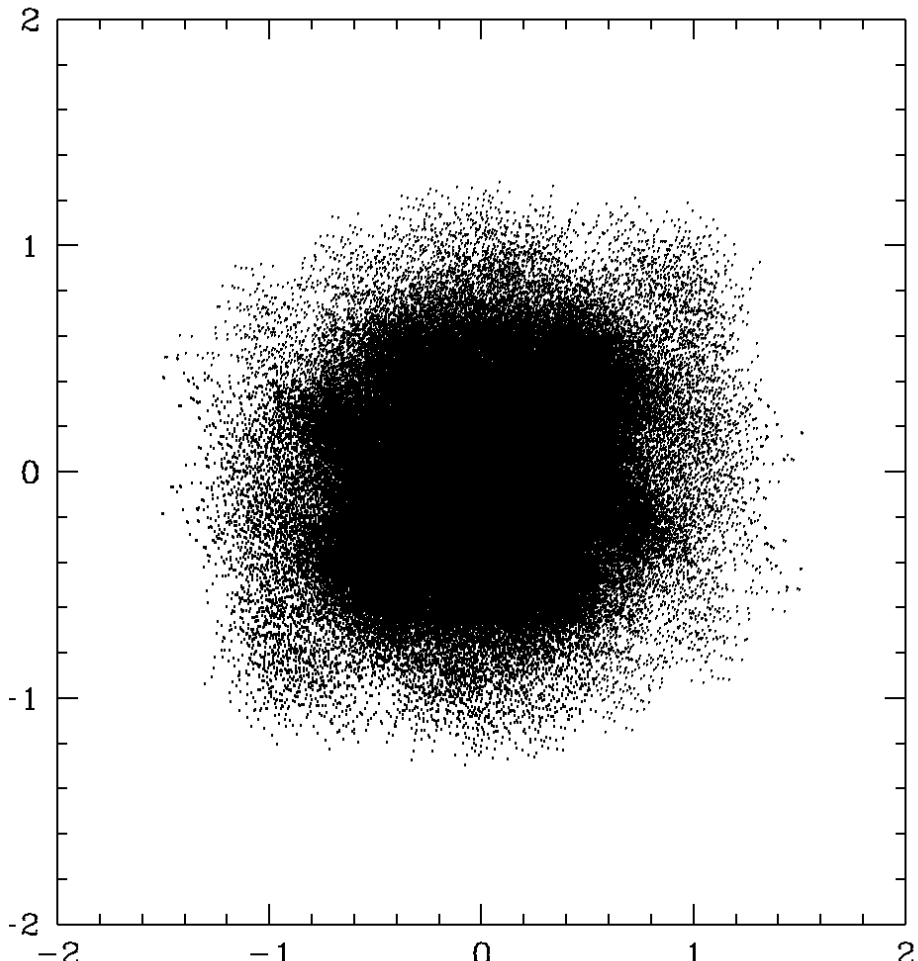
- Tiles scattered across 1.5 km region
  - Angular resolution: a few arcmin
  - Superb *instantaneous* PSF characteristics
  - Central condensation for sensitivity at large spatial scales
- Simplified design and operations
  - "Le mieux est l'ennemi du bien." – Voltaire
  - Campaign-based observing model
  - Affordable, focused operations

Physical Layout

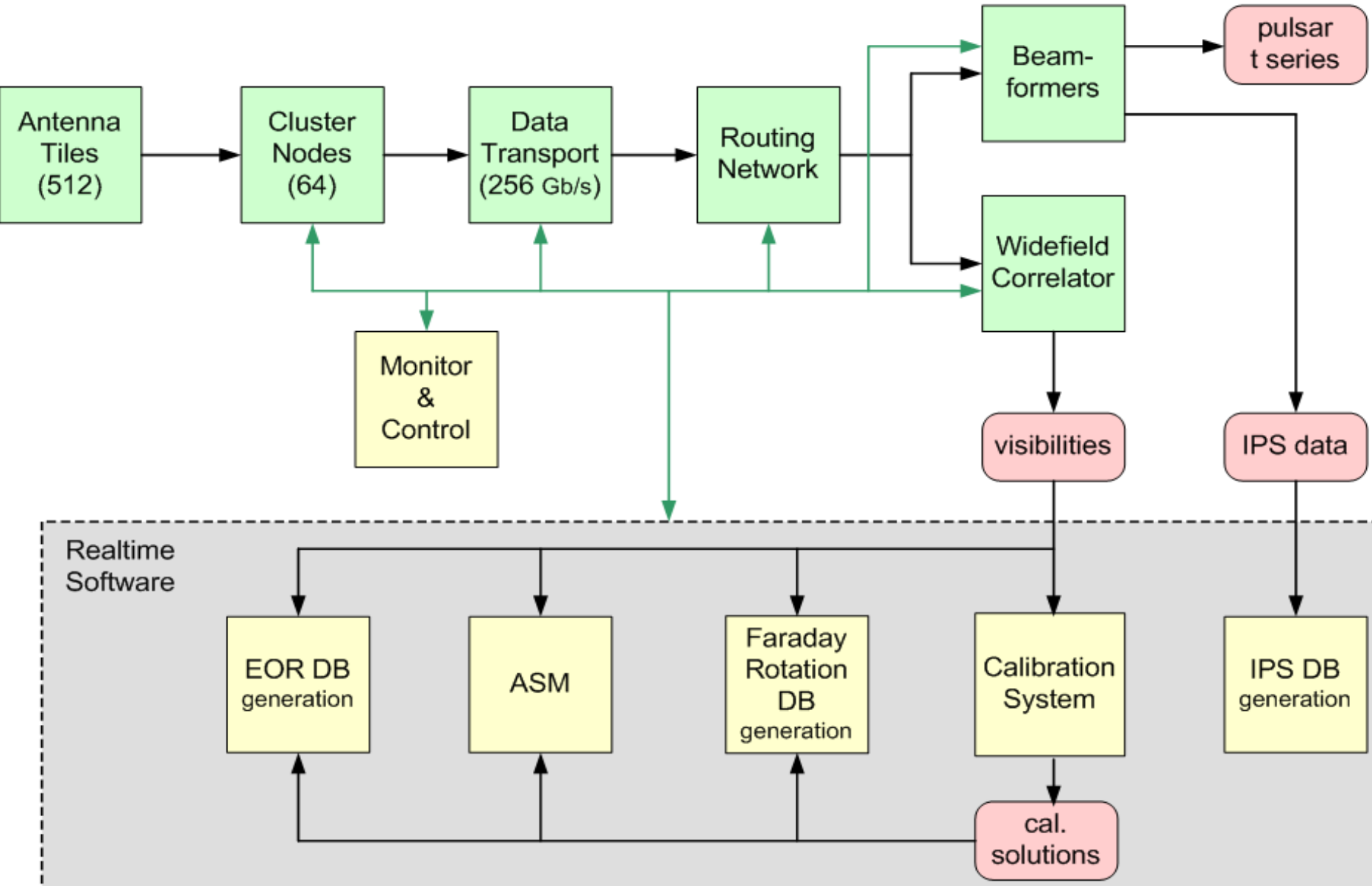


Configuration and UV Coverage





MWA System Block Diagram



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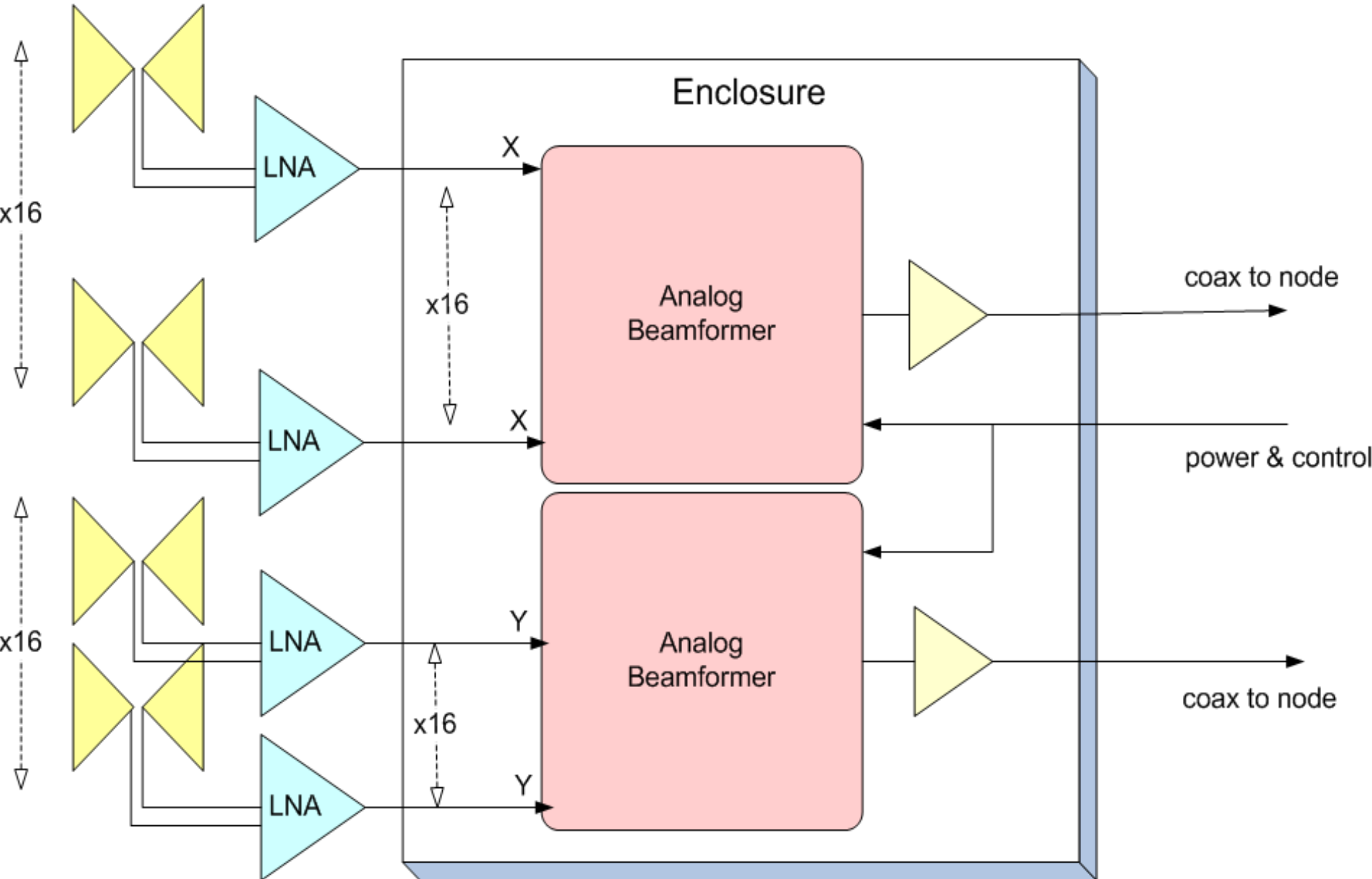
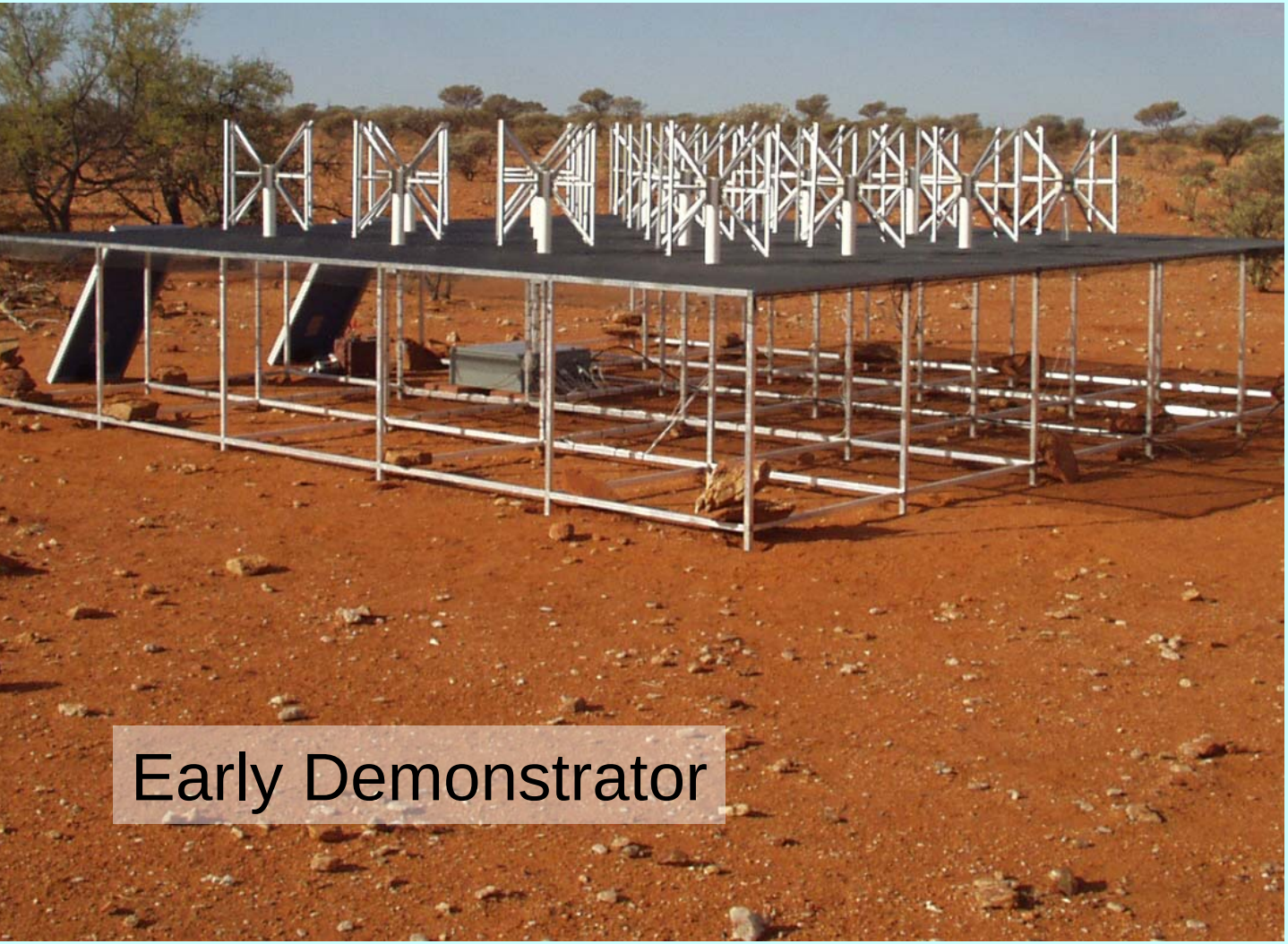
Antenna Tiles



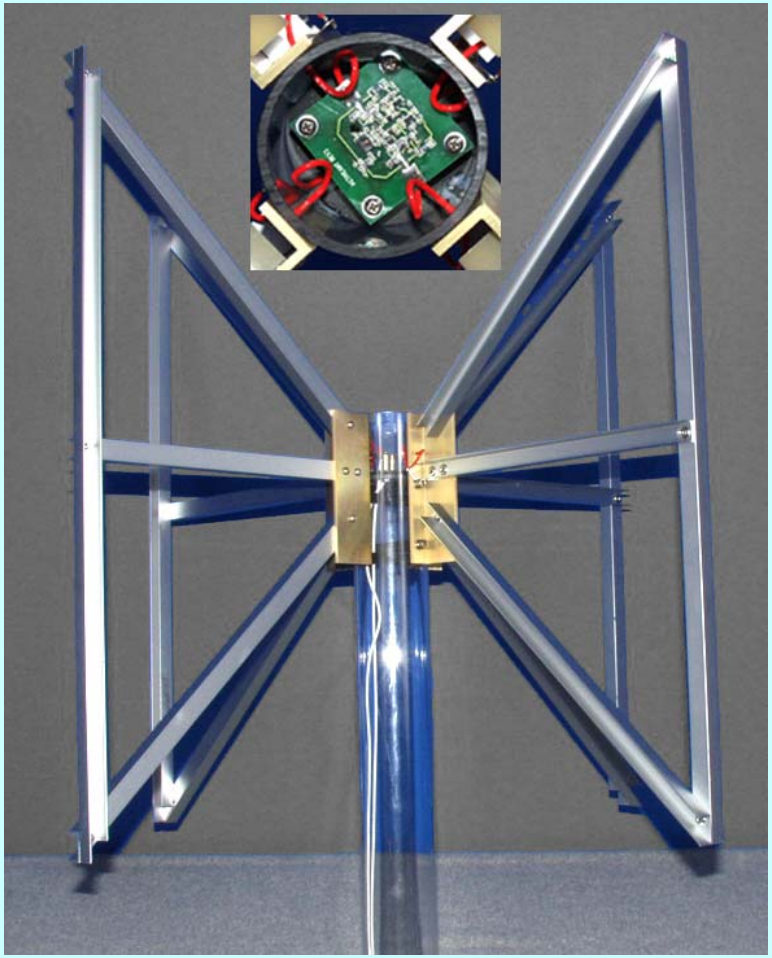
Tile Design

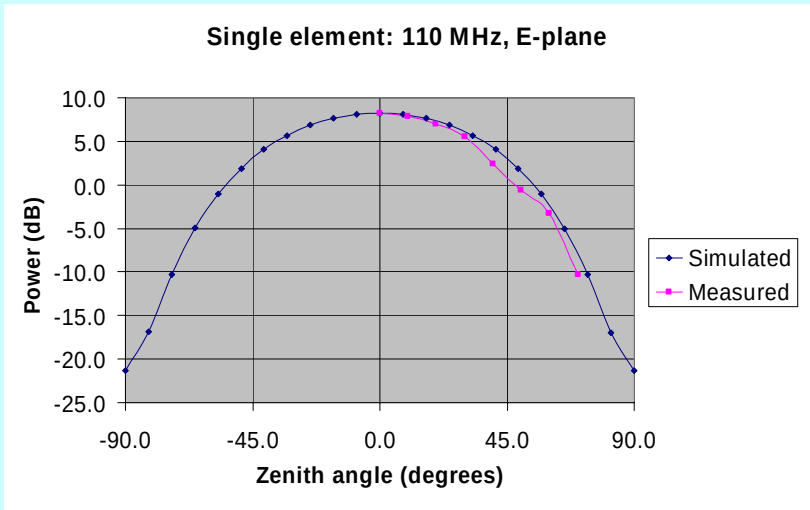


- 16 dipoles
- ~4m x 4m ground screen
- Dual-polarization
- 80-300 MHz
- Analog beamformer
- 30° min elevation

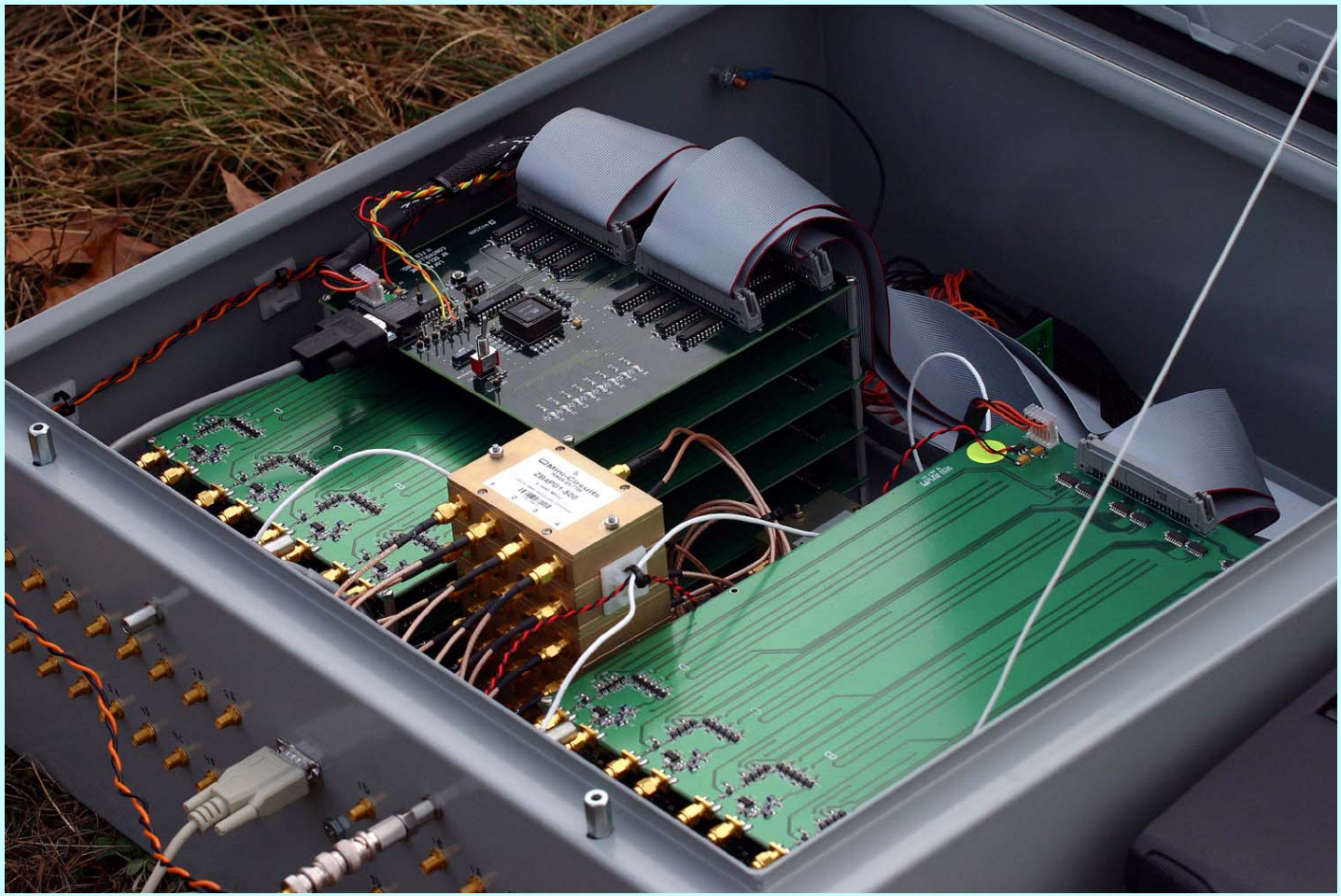
Target cost $2000 each

Crossed-dipole antenna prototype





Analog Tile Beamformer Prototype



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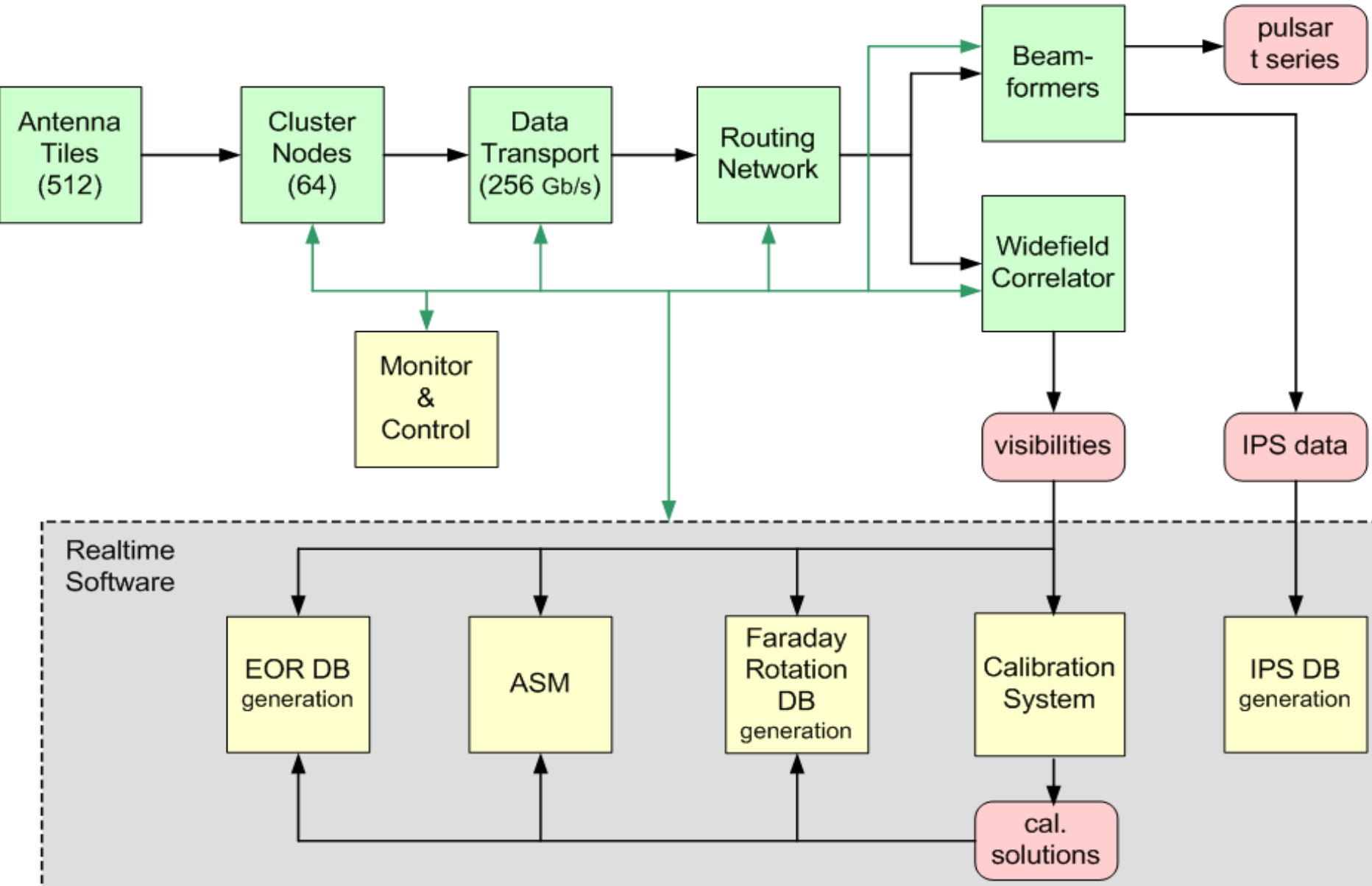

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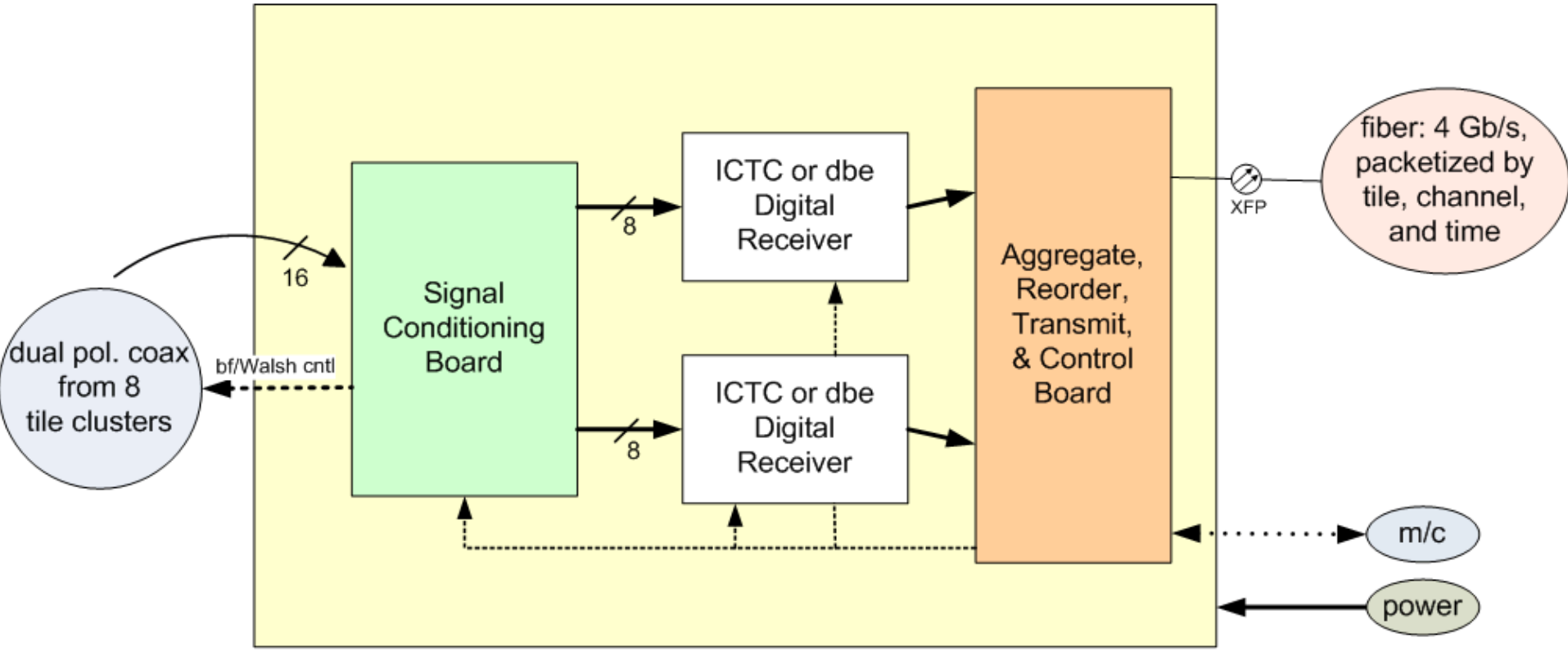
Cluster Node



Digital Receiver

- For each of 16 analog inputs, band from 80-300 MHz Nyquist sampled
- 1st stage filter bank (running at ~640 MHz) generates ~32 x 8 MHz channels, of which 4 are selected for further processing
- 2nd stage filter bank breaks each 8 MHz channel into 1024 channels of 8 KHz (memory issues)
- Complex spectral points are reordered, aggregated, packetized, and transmitted to the appropriate correlator slice

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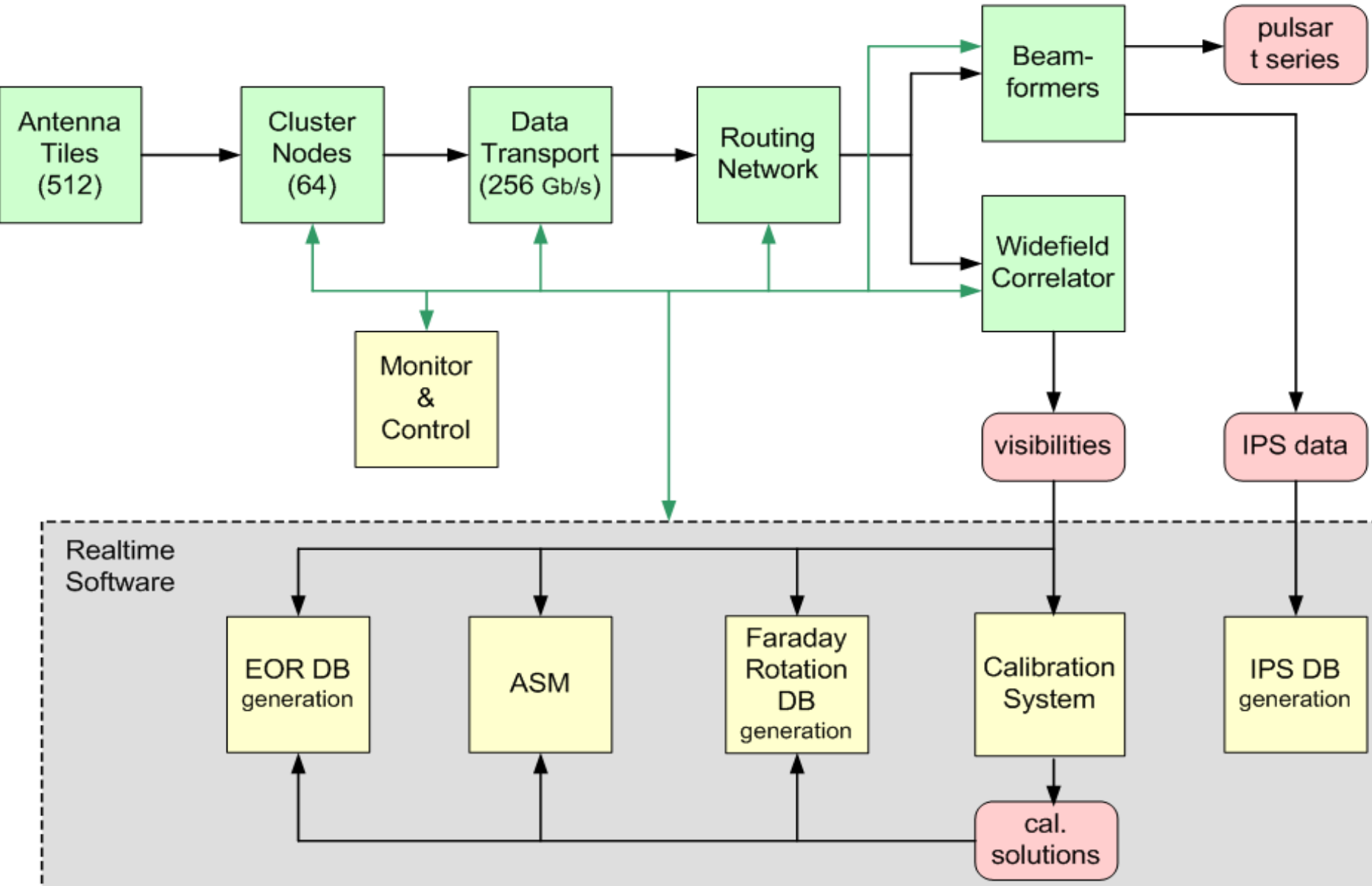

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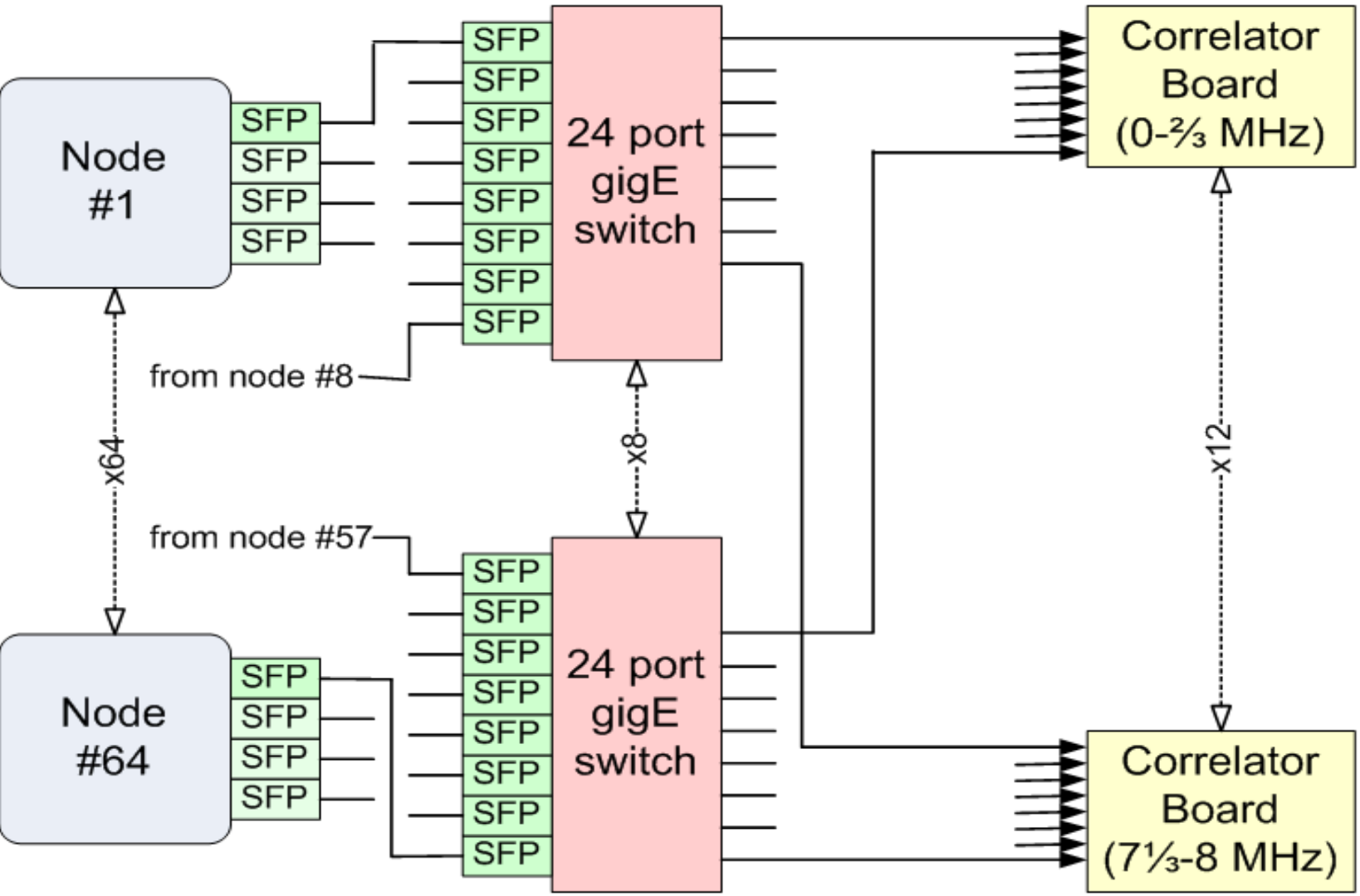
Transport Layer & Routing Network
8 MHz slice



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Widefield Correlator

- Cross-multiply of complex voltage spectra, without fringe rotation or gain correction
- 125K baselines x 4 pol's * 32 MS/s requires 16 TCMACs
- Plan to do complex (4bit) multiply in single multiplier
- Correlator is partitioned by frequency slice, into 32 – 64 boards, each processing 1.0 – 0.5 MHz of bandwidth, depending on efficiency of FPGA multiplier usage
- Local accumulation for 512 pts (64 ms), then LTA w/ RAM accumulates to 0.5s
- Yields 2×10^9 visibilities per 0.5 s AP dump
- 4×10^9 vis/s transmitted to realtime computer

Beamformers

- Form 16 beams
- Channelized to 8 KHz
- Arbitrary pointing, though sensitivity may be 20 or 30 dB lower outside of tile beam
- Linear combination of antenna signals and factors including gains, phase factor, weighting.
- Total computation ~ 0.5 Top/s
- Distributed across correlator boards

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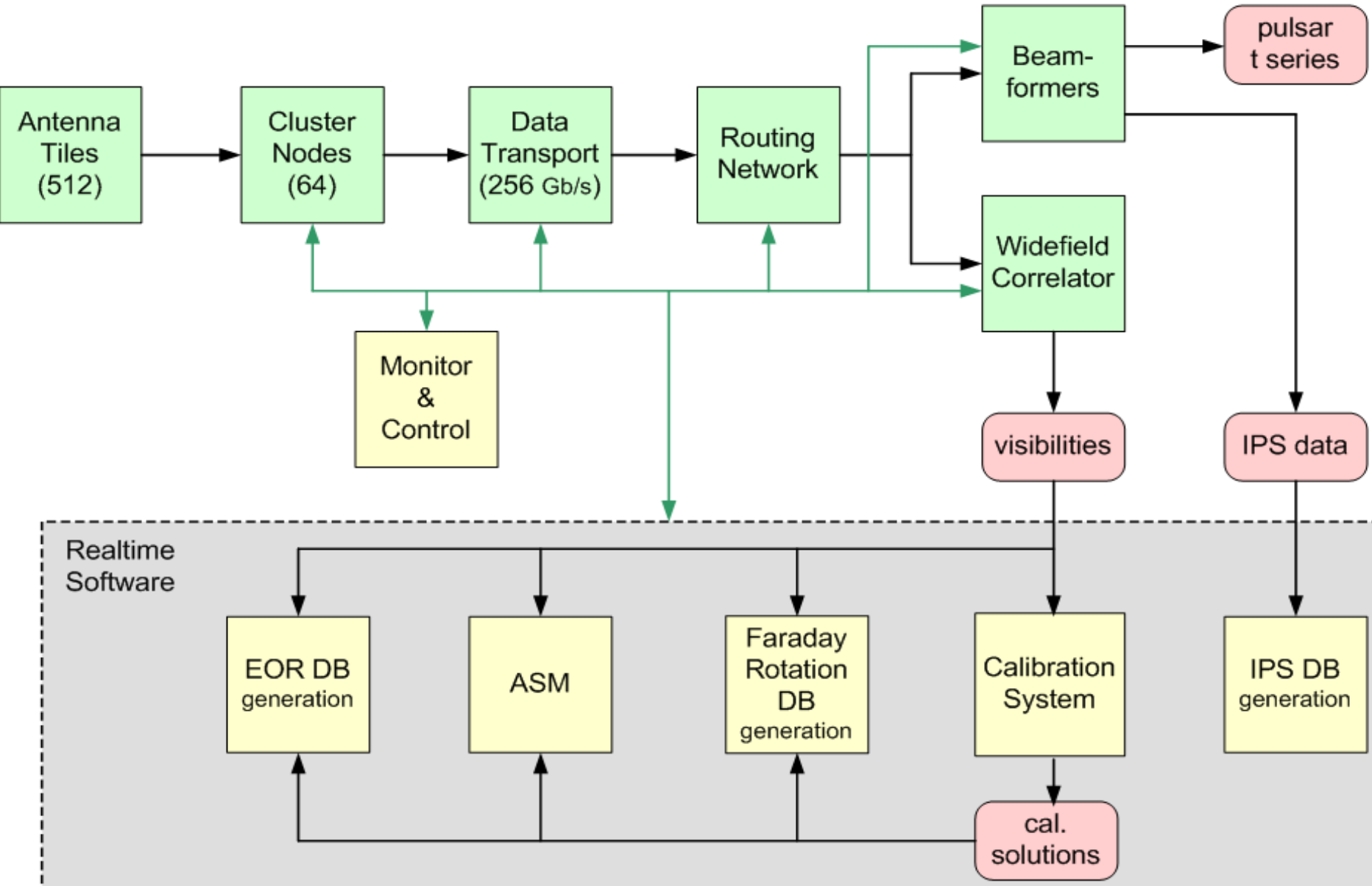

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Realtime Computer Specs

- Dataflow in:
  - Visibilities: 4×10^9/sec (128 Gb/s)
  - Beams: 512×10^6 complex samp/s (8 Gb/s)
- Internal dataflow:
  - ~30 Gb/s
- Computation:
  - ~80 Gop/s
- Computing environment:
  - At least 12 major apps with varied requirements
  - Must combine performance with flexibility
- Candidate system: Cray XD-1
  - Maximum computation per chassis:
  - Max. I/O bandwidth:
  - Approx. cost: