

Correlator Status

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Cast of Characters

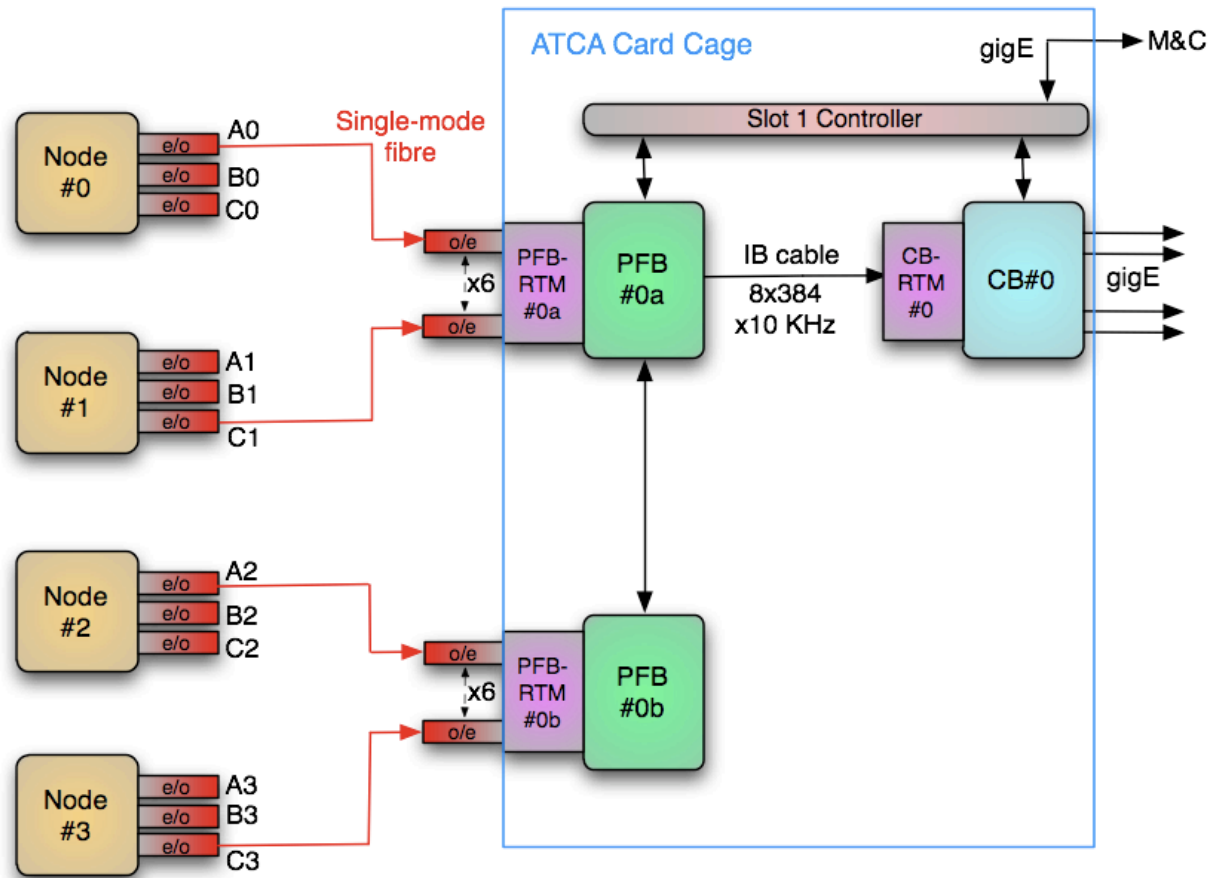
- **CSIRO/ATNF**

- Ludi de Souza - pfb firmware, board infrastructure firmware, development environment
- John Bunton - architecture, management
- John Tuthill - PFB/RTM design

- **Haystack**

- Bart Kincaid - correlator board firmware
- Russ McWhirter - pfb firmware integration, system integration
- Roger Cappallo - system integration, architecture, management

32T Digital Architecture



Hardware Status

- All 5 boards (PFB/RTM, PFB, CB/RTM, CB, Slot1) 100% functional
- CB received October, Slot1 controller just 2 weeks ago
- Inputs and outputs of CB & PFB are tested by Xilinx utilities
- FPGA - FPGA high speed serial paths tested by Ludi's software

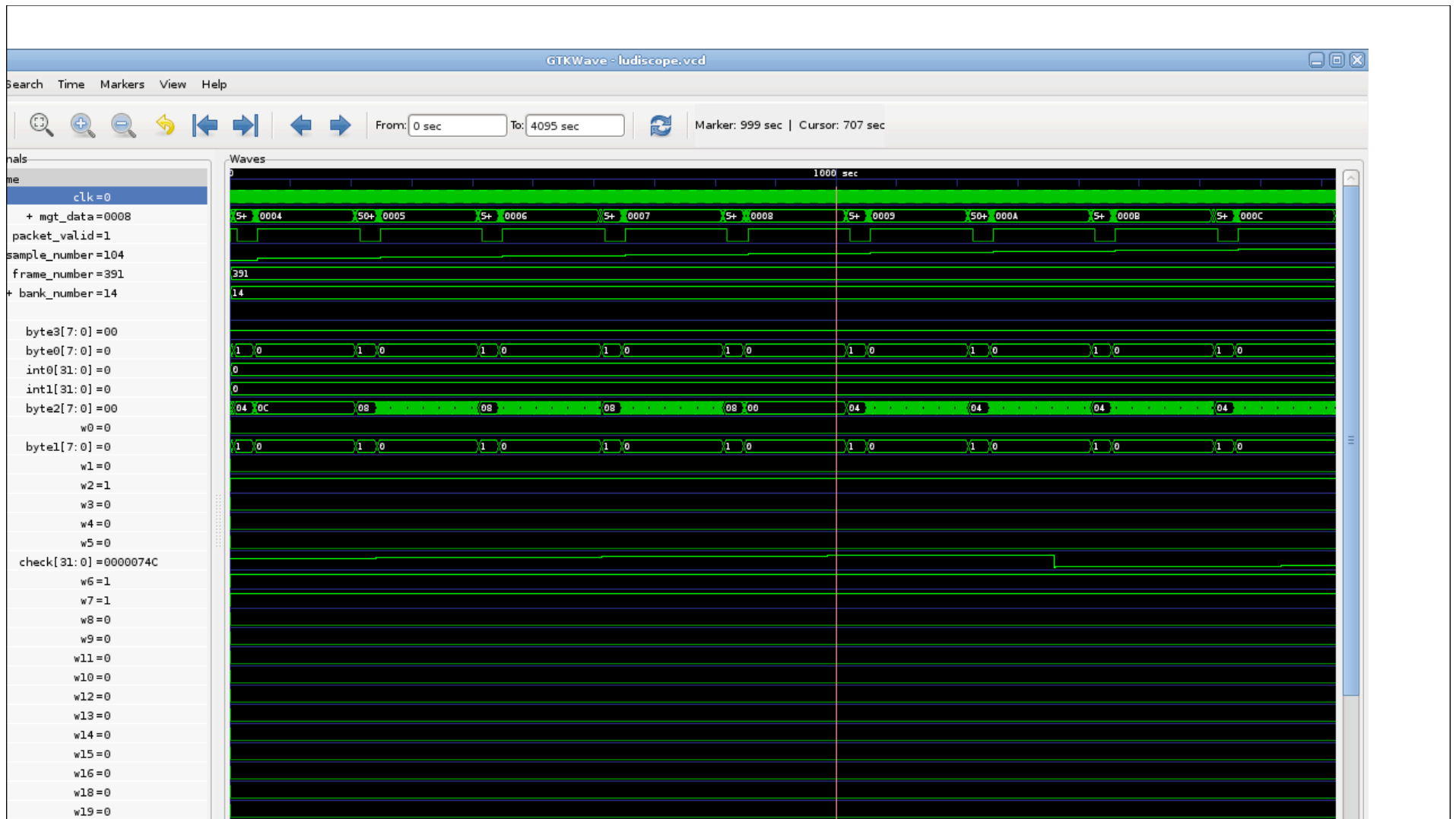


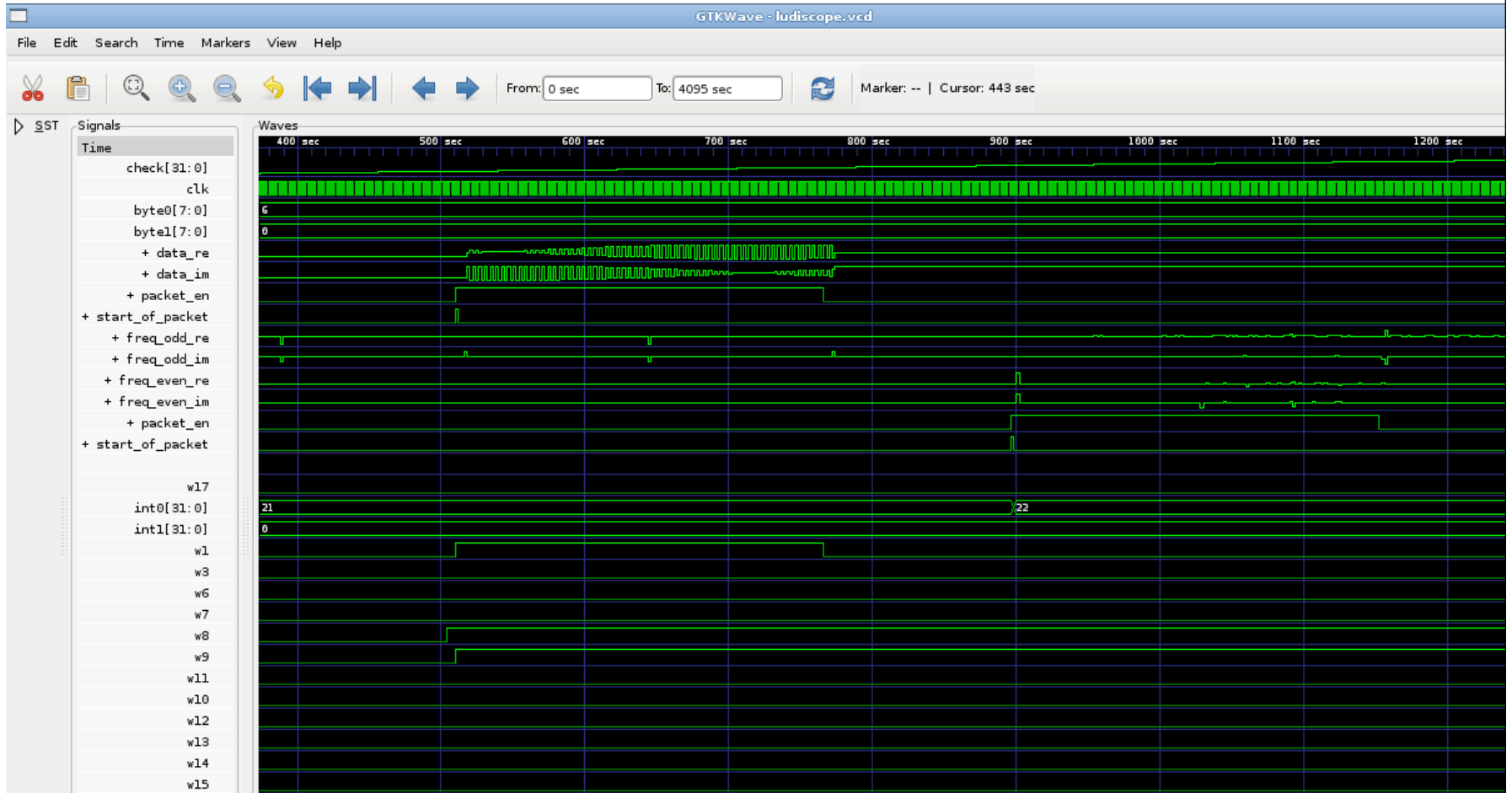
PFB Firmware Functions

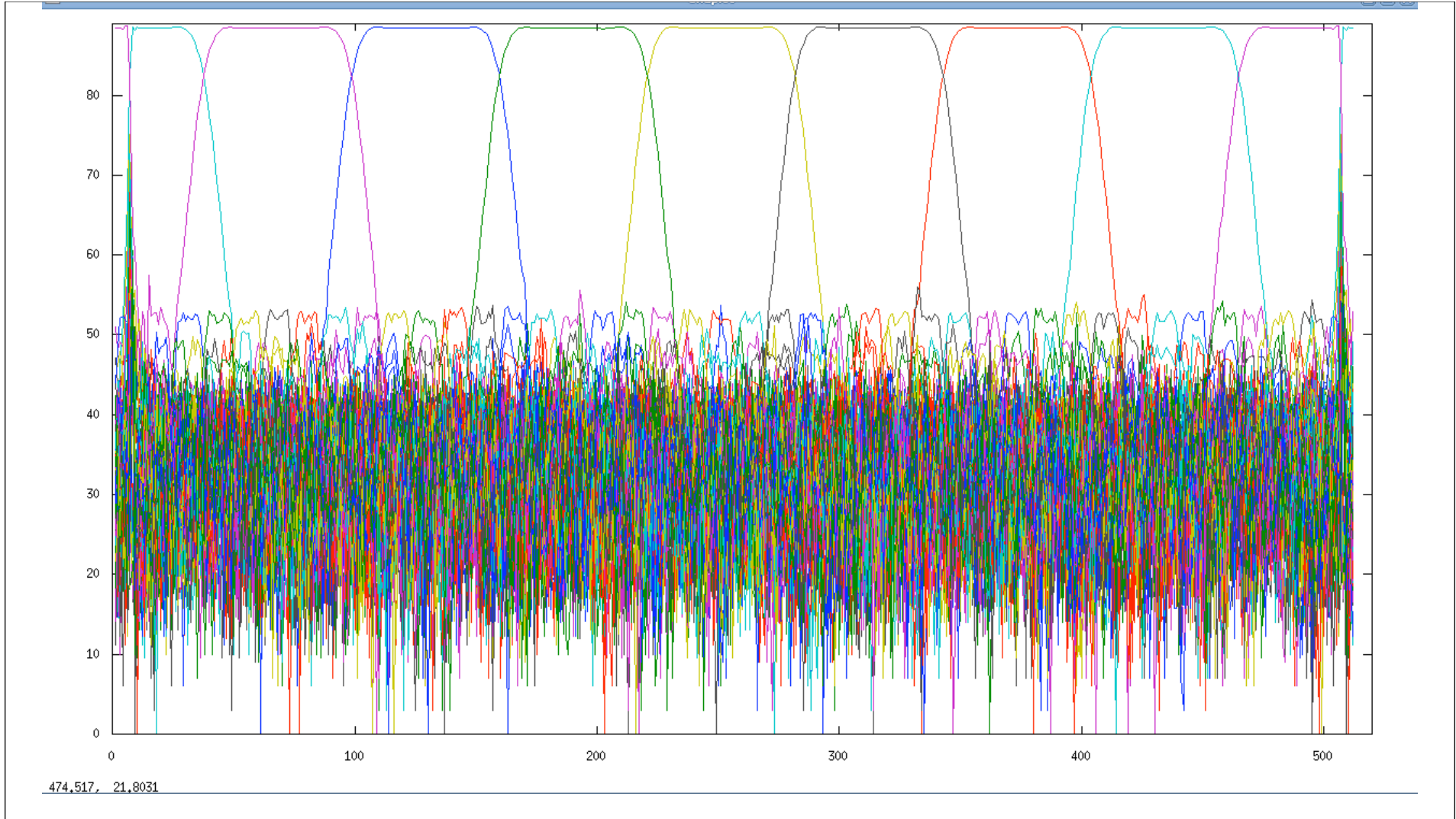
- Receive packets from receiver
- Deformat packets
- ICT: Reorder data for presentation to (time-multiplexed) pfb's
- Perform pfb's
- OCT: Reorder data into correlator order
- Format data into correlator packets
- Transmit packets via Rocket I/O MGT's

PFB Firmware Status

- All modules appear to be working - but separately
- e2e version with only 2 antennas of 1 coarse channel currently implemented for testing, with a simplified ICT, and all implemented in the (FX-60) INF chip
- data spot-checked to agree with simulation software; still need extensive testing
- about 1 month of effort remains to code full-width version
- full board will need to be used
- some slight concern about 300 MHz clock rate of memory controller







CB Firmware Functions

- Receive packets from PFB
- Deformat packets into data stream
- Route data to appropriate correlation cell
- Perform 500 sample complex cross-multiply and accumulate
- Combine four 10 KHz channels into one 40 KHz channel
- Format visibilities into UDP packets
- Transmit packets via gigE

CB Firmware Status

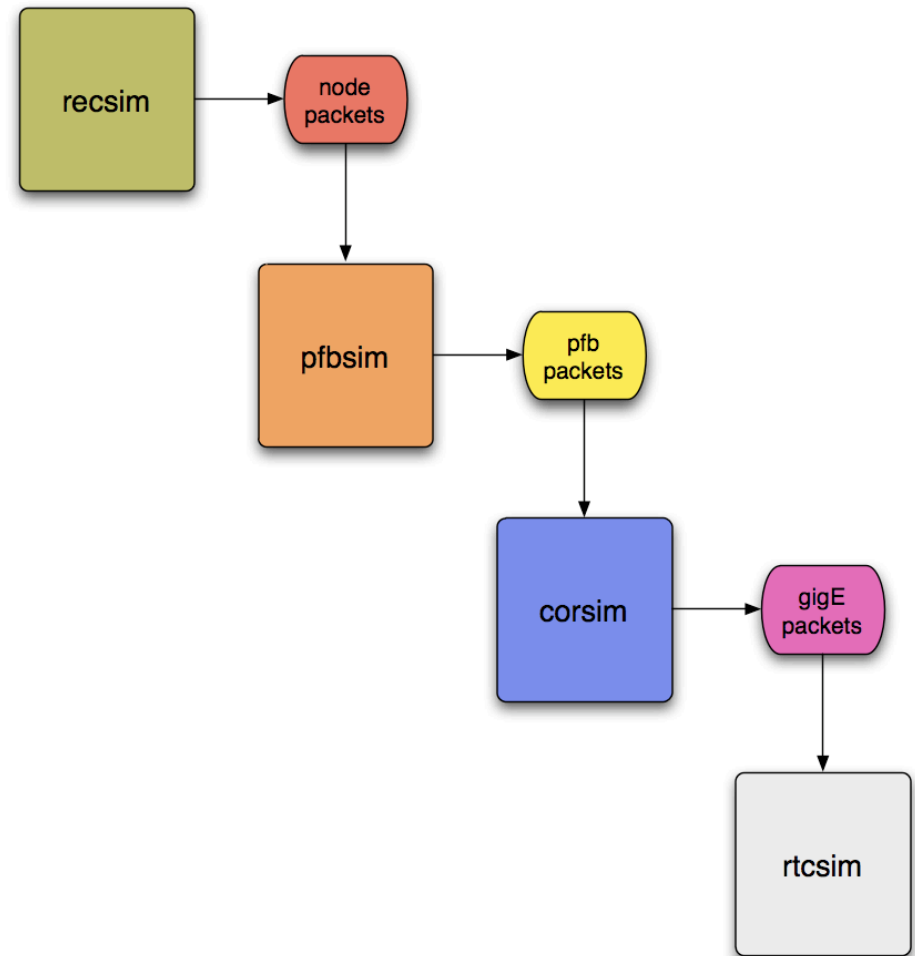
- Model of entire board “verified” by bit-level simulation in Spring 2008
- Received data and gigE output packets working correctly
- Problems with single-ended signal integrity necessitated change in approach
- Now using Ludi’s infrastructure for off-board and inter-chip communication
- Implemented as a wrapper around basic correlation engine components
- Allows superior debugging tools, and ease of M&C interface
- Time lost due to rewrite, as well as a few subtle problems caused by new paradigm
- Correlation cell once again working, rest of logic being re-enabled
- Full-width operation appears imminent

Rigorous Testing

- primary testing is via digital modules in a bit-by-bit comparison to software simulations
- will also inject analog signals into receiver as part of system integration activities
- code will be run continuously and results compared to reference output (some rtsim coding yet needed)

Software Simulation

- C programs to simulate and inter-compare to the bit level:
 - Receiver (AgFo) output
 - PFB board
 - CB board
 - RTC packet capture
- recsim & VHDL module generate:
 - constant frequency tone
 - frequency sweep
 - pseudo-random sequence



Contingency Plans

- **Decrease to 16 MHz bandwidth**

- Cuts pfb resource usage & memory rate in half
- Correlator board probably OK now, but this would also double the available CB resources

Deployment

- Ship ATCA card cage & 5 cards to Curtin
- Re-assembly & self-tests at Curtin
- Team of 2 +/- 1 from Haystack will accompany correlator for deployment activities

Beyond 32T

- **SKAMP**

- Near-term commitment to produce working 16 antenna prototype CB firmware
- Long-term commitment for full CB firmware

- **512T**

- PFB: need to add interconnect functionality across backplane mesh
- CB: need to fit 136 cells per CMAC, running at speed
- CB fallback - implement ~30 cells in an enlarged LTA
- Implementation of phased array beams